Real-Time Digital Signal Processing in a Mixed-Signal LSI Test System

In test subsystems based on digital signal processing, the HP 9493 test system emulates the analog and digital signals of the device under test, thereby reducing test time and increasing test coverage compared to a memory-based test system.

by Keita Gunji

Complex mixed-signal integrated circuits are used more and more frequently to realize many complex functions needed for applications such as telecommunications, servo control, and image processing. Testing of these ICs is much more difficult than for traditional ICs because of the integration of complex functions and synchronized interactions between blocks. Conventional IC testing methods cannot provide both high test throughput and high test quality for these devices. At-speed signal processing by synchronized distributed subsystems is required to perform functional testing of complex mixed-signal devices. Also required is a programming style that is straightforward and allows flexible control of signal and data flow in the test subsystems.

DSP-based LSI testers can be classified as having one of two types of architecture according to the location of the signal processing units (SPU): centralized or distributed. In the distributed type, SPUs are distributed among the individual subsystems. Usually, each SPU cannot manage a large amount of data and the processing speed of each SPU is slower than that of a centralized SPU. Programming is more difficult because the SPUs are not strongly coupled to the CPU, so the control layer between the CPU and the SPUs is more complicated. On the other hand, the distributed type makes it possible to process data in the subsystems and enables at-speed emulation of IC functions, which is required to test mixed-signal devices.

To meet the needs of complex mixed-signal testing, the HP 9493 mixed-signal LSI test system is based on distributed digital signal processors (DSPs). In each test subsystem is a Motorola DSP96002 chip, which runs at 32 MHz and performs 32-bit floating-point operations. The DSP modules are connected by data transmission paths for data sharing. A flexible programming language directs the DSPs to generate and analyze test signals.

The HP 9493 architecture allows digital and analog signal processing completion times on the order of microseconds to ensure the quality and throughput of dynamic signals and data operations for the device under test (DUT). Precise timing synchronization of all subsystems makes it possible to distribute operations among the DSP modules.

Compared to a memory-based test system, the HP 9493's distributed DSP architecture reduces test time and increases test coverage for complex mixed-signal devices. To generate an analog waveform, the conventional memory-based system must compute and store discrete time data for the entire waveform before generating it. This takes time and may require so much memory that the functions of a complex device may not be tested completely because of the memory cost. In contrast, the DSP-based HP 9493 prepares the discrete time data in real time using a much smaller amount of waveform memory.

Architecture

Fig. 1 shows the HP 9493 system architecture, which allows synchronous and asynchronous control of the analog and digital subsystems and the distributed DSP in each subsystem. This distributed architecture consists of a tester controller, which controls all test subsystems, a master clock subsystem, two test heads, and test subsystems. The test subsystems include digital subsystems, which generate and fetch digital patterns and signals, arbitrary waveform generator subsystems, and waveform digitizer subsystems.

In each test subsystem are a DSP module, a sequencer, and a memory block. Each DSP module has a data transmission path. The DSP modules operate on data or signals according to instructions loaded from the tester controller, and the start and stop operations are synchronized by the master sequencer or tester controller. The master sequencer precisely synchronizes the timing of the other sequencers.

The DSP96002 manages the memory block. Data can also be stored in high-speed memory in the DSP module to reduce memory access time, which increases the processing speed of the DSP96002. The sequencer in each subsystem controls address generation and the timing of data fetch or generation between the memory block and the signal input or output for memory-based testing.

The advantages of this architecture are real-time signal emulation and shared signal processing. Test throughput is more than double the capability of conventional LSI testers, and ICs can be evaluated at-speed functional tests. Data can be transmitted between DSP modules without CPU intervention, which allows synchronous and concurrent operation and sharing of signals from the DUT.

The DSP module in the digital subsystem can fetch and generate up to 32-bit digital test data. The test data is directly connected to the data bus of the DSP96002. Data can be
Fig. 1. The HP 9493 mixed-signal ISI test system architecture puts a local DSP module in each test subsystem.
transmitted between the master and slave subsystems on a per-pin basis. This is necessary for high-pin-count devices or multidevice testing. The number of pins can be expanded to 256. The analog subsystems are connected to another data transmission path to enable real-time data transmission across subsystems while testing.

The DSP module in the waveform digitizer fetches and processes real-time or buffered sampling data, and can transmit data to other subsystems and the digitizer memory block. Real-time processing and a memory interface allow the capture of DUT responses or signals without restarting the test sequence. This is useful to emulate functions such as ISDN activation. Conventionally, another ISDN device is used to generate the signals required for testing this function, but this method does not have the flexibility to accommodate changing test specifications. Emulation of the activation sequence also allows complete control and synchronization with the tester during the test sequence, which is difficult with an actual IC. A memory-based test system would require over 20 Mbytes of waveform memory to emulate this function. In contrast, the HP 9493 can do it with a maximum waveform memory size of only 2 Mbytes.

The DSP module in the arbitrary waveform generator fetches data from the waveform memory or another DSP module. Waveform data can be generated using a convenient waveform editor, loaded from the CPU directly, captured by the digitizer subsystem, or fetched from the digital subsystem.

**DSP Module**

Fig. 2 shows a block diagram of the DSP module. Synchronous lines controlled by the master sequencer are connected to the DSP’s interrupt and the subsystem’s acquisition strobe, allowing synchronous or coherent signal processing across subsystems. The synchronous trigger lines start operations of the subsystems and DSPs.

A test program in the DSP module must run an initialization process for any variables and global setup and cannot start with the timing of this trigger line. For complete synchronization, the DSP96002 is controlled to wait for an acquisition strobe at its acknowledge input before doing any data sampling or generation. DSP data acquisition is synchronized with the DUT by this acknowledge line. The acknowledge line is connected to the sequencer and the acquisition strobe to enable full synchronization of all DSP modules within one DSP cycle.

For digitizing, initialization starts before real-time data sampling. The acknowledge control waits for the acquisition strobe of the digitizer before moving data from the digitizer to the DSP. After the initialization of a test program, if the user starts a digitization, the DSPs get data from the beginning of sampling synchronized with the strobe. Synchronization is required to analyze vector data such as the I (in-phase) and Q (quadrature) outputs of a π/4 DQPSK device accurately.

For waveform generation, the sequencer halts data movement from the DSP while the sequencer is generating data to the DAC. It can switch data between the DSP and the waveform memory during an acquisition cycle. The waveform in Fig. 3 shows an example.

The acquisition strobe timing of all of the digital and analog subsystems is accurately managed at the DUT pins. Synchronization accuracy on the order of 100 ps is maintained.
The data transmission paths allow data transmission between subsystems for synchronized interaction, and are also used to synchronize the distributed DSPs with an accuracy of one DSP clock cycle. These paths conform to the RS-422 standard. The test subsystem grounds are isolated to reduce noise transmission.

Software
The usual problem with a distributed system is the complexity of the control layer from the CPU and the fact that the signal processing function cannot be controlled directly by the CPU. To test various chips, the test system software should be flexible enough to execute any DSP program. Easy programming is required for the inputs and outputs of the test subsystems. The HP 9493 software hides the complexity of hardware control, and uses a programming style based on signal analysis using data flow diagrams, which consider signals and data flows in the test system. This programming style separates system hardware control and low-level DSP programming so that DSP algorithms can be developed independently of the tester.

Modular Operation Library. Conceptually, the test system hardware can be represented by a data flow diagram as shown in Fig. 4. Each operation shown in Fig. 4 can be described as shown in Fig. 5. Each operation has inputs and outputs, and the user can switch the I/O and execute the same operation using different subsystems. The HP 9493 test plan language controls the loading of the operation and the I/O connections. Using this conceptual model, the complexity of hardware control can be hidden by the software, so that programmers only need to define the input and output relationships between operations and test subsystems.

For operations that are signal processes such as filtering, algorithms can be programmed using the DSP’s assembler and compiler without considering the hardware subsystems.

Test Plan Language. A test plan language is supplied to create test sequences for the HP 9493 test system (see Table I). Programming is based on the data flow diagram.

<table>
<thead>
<tr>
<th>Function</th>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOAD-MOL</td>
<td>PIN LABEL MOL</td>
<td>Selection and loading of an operation library</td>
</tr>
<tr>
<td>SET-MOL-MODE</td>
<td>PIN OPERATION-MODES</td>
<td>Definition of the operation mode of the DSP module</td>
</tr>
<tr>
<td>SET-MOL-IO</td>
<td>LABEL INPUT OUTPUT</td>
<td>Input and output definition of the operation library</td>
</tr>
<tr>
<td>SET-MOL-ARG</td>
<td>LABEL ARGUMENTS</td>
<td>Setting of the arguments of the operation library</td>
</tr>
<tr>
<td>READ-MOL</td>
<td>PIN NUM-OF-ARRAY</td>
<td>Reading of output from the operation library</td>
</tr>
</tbody>
</table>

The test plan language can be used to execute any function and makes it easy to create functional tests using the DSP capabilities in the HP 9493 test system.
Conclusions
The HP 9495 mixed-signal LSI test system contains high-performance digital signal processing modules in each test subsystem. This allows data processing with synchronous interaction for at-speed functional testing of mixed-signal devices. A programming language for test library development is provided by the system software. This helps develop and execute functional tests of various mixed-signal devices.

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Reference