

Developing a Design for Manufacturability Focus

The HP Australian Telecommunications Operation has rapidly evolved from a custom test instrument developer to an operation that develops and produces products in higher volumes. Significant cultural and technological hurdles have been overcome during the transition to an operation focused on design for manufacturability.

by **John G. Fuller**

The need for organizational change can be driven by many factors. In the case of the HP E5200A broadband service analyzer, the HP Australian Telecommunications Organization (ATO) intended to address a different market through a significant step forward in product technology.

ATO's first product was a custom digital performance monitoring system, delivered during the late 1980's. ATO had also recognized an immediate market need for high-performance SONET/SDH (Synchronous Optical Network/Synchronous Digital Hierarchy) test instrumentation, and in 1990, began work on the definition of a VXIbus test system. This product was delivered in the second half of 1991.

These first ATO instruments were largely based upon through-hole manufacturing technology. They used some surface mount technology for the high-speed interface connections to customer equipment. The technologies did not present a difficult manufacturing problem and the testing approach was largely of a functional nature, with some external fault diagnostic tools being developed by ATO manufacturing engineering. These tools consisted of field-programmable gate array (FPGA) configurations that could be used to test the large amount of digital interconnect within the product. Shipment volumes were low enough to be handled by a very small production group which outsourced assembly work wherever possible. It is worth noting that the marketing planning, development, and manufacturing design were done concurrently. This led to a relatively short time to market and provided ATO with a sound cultural basis for future concurrent development of new products.

The next couple of years saw very little change in technologies or volume. Essentially, ATO was making printed circuit assemblies that were easy to build, dealing with product volumes that didn't demand an abnormal amount of effort in design for assembly (DFA) or design for test (DFT), and scrapping the occasional printed circuit assembly that defied all attempts to make it work.

This approach was far from the optimal situation for the manufacturing group, but it was manageable and paid dividends in terms of ATO's profit line and growth. The down-side of the equation was that, while concurrent engineering was being used to some extent during this time, a culture evolved that tended to minimize manufacturing involvement in the design process. This reduced the manufacturing contribution to the design process and limited the interaction between hardware designers and manufacturing engineers. While many reasons for the reduced involvement could be suggested, we feel that the most likely cause was that a lack of product technological change led to less emphasis being placed upon development and manufacturing process improvements. This also led to more emphasis being placed upon manufacturing contributions to functional and quality assurance testing during development. Thus, ATO's manufacturing staff was more involved in the test process than the development process while operating within a low-volume, high-cost, high-mix, and relatively high-profit manufacturing environment.

It is from this cultural atmosphere that ATO's strategic direction shifted away from the R&D market toward the installation market. Associated with the shift was a market requirement to reduce both the size and cost of our product without detracting from its performance. Thus, ATO's manufacturing group was gazing down the development pipeline at a high-technology product that would lead to significant increases in volume, lower selling prices, and eventually, lower profit margins. Clearly, these were very good reasons why change was seen to be necessary.

What Needed to Change?

Having established the need to change, it was necessary to evaluate what processes would have to change to meet the needs of the new marketplace. These were seen to be largely driven by the expected technology leaps in the new product, the volume increases, and the lower profit margins that were expected. Time to market was also seen as a critical factor that had to be minimized in every way possible.

The technological issues were of great significance. ATO was moving from product platforms based largely upon through-hole technology to platforms based largely upon surface mount technology. Worse (or better?) still, the use of surface mount technology was expected to be extreme, with the main printed circuit assembly (400 mm by 230 mm) carrying over 1000 components needing almost 8700 solder joints spread over both sides of the board. The degree of difficulty associated with the solder joints was also of significance: approximately 4500 of them were expected to be extra-fine-pitch (XFP) at 0.020-inch spacing with a further 900 expected to be fine-pitch (FP) at 0.025-inch spacing. A difficult task even for a world-class manufacturer!

Aside from the technology issues, it was also apparent that the small size of the printed circuit board would seriously limit the amount of physical test access, thus requiring an innovative testing approach. With approximately 3000 electrical nodes and access to about only 600 of these because of space limitations, it was clear that diagnostics in the production area (and later in the field) were going to be of paramount importance. Additionally, each printed circuit assembly was expected to have a significantly high component cost. It was never going to be an option to simply scrap the boards that were difficult to repair—a daunting thought when ATO's estimates were predicting around one defect per board after in-circuit test at the manufacturing center!

With the ability to accurately diagnose, test, and assemble the product being so vital to manufacturing success, it was quite apparent that manufacturing engineering teams responsible for materials, test, process, and regulatory functions would need to form and maintain a close alliance with the hardware and software design teams. This would require organizational efficiencies and working relationships, particularly between R&D and manufacturing, on a scale not seen before at ATO. Development cycles would need to shorten still further, placing additional pressure on all aspects of the organization's performance. Effective teamwork and communication skills would have a major impact on the overall success of the product.

In summary, major technological and process improvements would be required, as would significant cultural and behavioral shifts within the organization, to support the technical changes.

Managing the Change

To produce the required technological and process improvements, manufacturing engineering needed to develop a thoroughly different core focus from doing QA testing in parallel with other manufacturing tasks. It was recognized that a significant contribution to the design process could be achieved only by manufacturing engineers becoming more specialized and focused upon particular job functions. Technically, this meant that as manufacturing engineering functions such as test, process, regulatory, and materials became adequately skilled, it was possible to increase the manufacturing contribution to the development process. This ultimately led to a closer involvement with design teams at a much earlier stage in the product life cycle.

Manufacturing targets also became a more important part of the design process, so that measurement of the cost drivers associated with building a product were given more visibility during the early development stages. Manufacturing engineers initiated a sustained effort to review design for manufacturability (DFM) issues, set appropriate assembly, test, and diagnostic targets, and then provide regular feedback into the development process. All the manufacturing engineering functions mentioned previously were involved, an excellent example being the EMC design process (see *Subarticle 12a*). The manufacturing processes were also subjected to the same kind of scrutiny. Clear targets were assigned for each station in production, and engineering owners were responsible for driving their station toward meeting targets, thus enabling a subsequent handover to the production staff.

With the sharpening of focus on materials, regulatory, process, and BIST (built-in self-test) engineering functions, there was a need for increased contact with the hardware and software designers. This required a significant effort in terms of teamwork and communication skills, and a cultural shift at both the manufacturing and R&D ends of the development process. For example, as manufacturing engineers prepared to contribute to the design process with manufacturing inputs in a way that would benefit the design process and the manufacturing function, designers also had to prepare to take and constructively question the inputs provided by their downstream customers. A cultural shift of this nature does not happen easily and it required an environment of significant trust, teamwork, and communication that was developed over a period of time. The objective was for manufacturing engineers to become design-capable partners for development who can continually improve the DFM process.

Development partnerships were also used to great effect in other areas. ATO has been working successfully with HP's Surface Mount Technology Center in Spokane, Washington for several years. The Surface Mount Technology Center was heavily involved in the surface mount process development and the in-circuit test development for the service analyzer product. Manufacturing partnerships for the plastic components (cases, handles, feet, etc.) and the aluminium die-cast pod casings also made a significant contribution as ATO began to use unfamiliar technologies. As a result of the service analyzer project, a strong emphasis is now placed on the benefits of concurrent engineering involving HP partners inside and outside ATO, and on working closely with partners outside HP.

Many concurrent engineering best practices have been learned during this product development, with major benefits being derived from:

- An emphasis on teamwork and communication skills by everyone involved

- Early and regular involvement throughout the product life cycle by all groups and individuals charged with contributing to that development
- An emphasis on contribution to the design process rather than limitation of it
- Continual improvement of the product life cycle process through critique of the concurrent engineering effort.

Technical Changes

Many technical changes were necessary as a result of ATO's new direction. Broadly speaking, the technologies involved in the service analyzer project drove significant surface mount process changes (see **Subarticle 12b**), manufacturing engineering process changes (which were addressed by a sharper focus of engineering resources), and major testing challenges.

The testing challenges were posed by the high component and pin counts, the multiple-CPU configuration, the lack of available test points, the high component costs, and the expected degree of difficulty involved in fault diagnosis. It was forecast that these boards would be of a significantly higher volume than anything else that had been manufactured previously by ATO. These volumes were considered relative to the issues mentioned above, and other factors such as head-count limitations, repair and diagnosis times, inventory, test equipment, and expertise required of technicians. It became very clear that an innovative test approach would be necessary to avoid a sustained engineering involvement in the repair and commissioning process.

Boundary scan (IEEE 1149.1) was the chosen test technology, and its extent and use were largely determined by the expected low number of physical test points on the board. It was linked to a detailed built-in self-test strategy that involved an extensive hardware, firmware, and software effort.

With the available physical test access diminishing during the development process (rather than increasing), a large emphasis was placed on getting access through substitution of boundary scannable components wherever possible. This approach eventually covered some 65% of the electrical nodes, with additions being mainly in the area of glue logic, since the ASICs and FPGAs were already scannable. Manufacturing's view of the potential diagnosis issues made the additions well worth the extra cost of the components. The printed circuit board real estate taken up by the extra pins was far less than the space that would have been taken by physical test points, thus providing the printed circuit board designer with more flexibility.

Test Strategy

The overall testing approach can be summarized as follows (see **Article 13** for more details):

- In-circuit test was used at the Surface Mount Technology Center after the boards were loaded, with physical test access being supplemented by boundary scan vectors on the Hewlett-Packard 3070 board tester wherever possible. Sufficient test points were placed on the printed circuit board to allow the scan chain to be broken into convenient chunks to aid in debugging and running tests. One of the design trade-offs included a decision to restrict in-circuit test access to some areas of the board. This was primarily driven by a lack of scan capability and layout difficulties in some of the RAM circuits. The rationale behind this potentially risky decision was that inspection at the Surface Mount Technology Center would pick up any obvious manufacturing defects, and built-in firmware test should specifically confirm the functionality of these areas at ATO.
- Extensive scan testing was used at ATO through the IEEE 1149.1 test access port (TAP). This was done before loading any software or firmware on the printed circuit assembly. It uses high-resolution vectors that are generated and inserted by a PC-based system. Automatically generated vectors are coupled with manually generated cluster test vectors to maximize the available scan coverage. This approach was intended to be a good fault resolution and diagnosis tool. However, more work still needs to be done to determine the overlap with scan testing at the Surface Mount Technology Center. When this paper was being written, the PC tools for insertion of the vectors were fully developed and the additional test and fault coverage was considered to be worth the increase in run-time overhead in the manufacturing process.
- Firmware access to the scan chain was made available through a test bus controller IC, which allowed firmware insertion of high-coverage, low-resolution built-in self-test vectors from the service analyzer hard disk. This test ran automatically (and very quickly) at power-up and communicated simple pass/fail results to a four-character alphanumeric display on the printed circuit assembly. A major advantage of this approach is that new vectors can be added to the hard disk or modified when test deficiencies are found during normal production.
- Some very extensive functional testing also runs from the firmware at power-up and includes at-speed tests of various functional blocks within the product. Checkerboard testing of RAMs and microprocessor communications ports, and staged loopback (transmit to receive) tests, are just part of what has been a significant software and firmware attempt to provide built-in, high-resolution diagnosis capability in the service analyzer. All of these tests can be run individually in a postmanufacture (service) situation.
- The final test approach used in production applies mainly to the parametric aspects of the product—for example, the optical and electrical connections to the outside world. A more traditional (minimized) functional

test method is used here with calibrated equipment and gold standards being used to verify that the product meets the published parametric specifications.

Results

From our manufacturing viewpoint, many breakthroughs were achieved during the development of this product. Perhaps the most obvious would be the technological leaps forward. The hardware components that were selected led to a significant extension of the Surface Mount Technology Center manufacturing and test processes. At ATO, the DFM process is considered to be vastly improved and is expected to be a significant contributor to the success of future projects.

In terms of the bottom line, the question should be asked, "Was the result worth the effort?" This is always a difficult question to answer when a specific measurement has not been defined for intangibles such as working relationships. We are of the opinion that the improvements that have been made in working relationships between R&D and manufacturing have made the effort well worthwhile. However, there were also other, more definable results such as:

- A minimal increase in costs for scannable glue-logic parts
- An increase in available printed circuit board real estate as a result of the minimized requirement for physical test access
- Reduced manufacturing test and fault diagnostic time
- Minimized effect of prototype and pilot build times on time to market
- Reduced impact on development work as a result of R&D involvement in resolving manufacturing defects.

When these results are considered along with our ability to make far better use of these tools next time around, the question becomes much easier to answer in the affirmative.

Acknowledgments

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