

Implementation of Pad Circuitry for Radially Staggered Bond Pad Arrangements

One approach to pushing the limits of wire bonding pitch in IC packages is to use two rows of radially staggered bond pads. This paper discusses the design of pad circuitry to mesh with the radially staggered bond pad arrangement. A test chip that incorporates suitable test structures was designed, fabricated, packaged and tested to verify the viability of the approach.

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Assembly and packaging technologies are major contributors to the success of integrated circuit manufacturing. With increases in silicon density, chip core sizes are shrinking with the minimum transistor size. However, I/O pad circuitry and size are not shrinking relative to core size because of packaging limitations such as capillary interference, long wires, wire sweep problems,[†] and corner crowding. There are a few workaround techniques such as wedge-wedge bonding and double-tier bonding which are available for the more expensive packages like PGAs. However, these techniques are unsuitable for standard plastic packages. There is need for a better, more reliable, and more cost-effective solution to the bonding pad pitch problem in the near future as more IC chips are becoming pad-limited.

The pad-to-pad repeat distance on a chip, referred to as wirebond pitch, is often the factor that limits both the amount by which the chip size can be reduced and the increase of I/O density, thereby reducing the efficiency of silicon area utilization. Current practice allows minimum straight-line pitches to be in the range of 100 to 125 micrometers. In [Article 6](#), one approach for decreasing the wire pitch in IC packages is discussed. This approach entails the use of two radially staggered rows of pads on the chip periphery as opposed to the more conventional single-row, inline arrangement.^{1,2} The bond pads are arranged to ensure no overlapping of bonding wire trajectories, even when conventional leadframes are used for the package. The radially staggered arrangement of bond pads allows uniform placement of wire trajectories despite the geometric fan-out from the die bonding pads to the leadframe bonding fingers. This approach is advantageous because it circumvents the common obstacles to fine-pitch bonding, such as capillary interference, bond placement accuracy, and wire size reduction, which have heretofore proved to be insurmountable.

This paper summarizes the main features of the radially staggered approach and discusses its implications for pad circuitry design. The implementation of radially staggered bond technology presents technical challenges in the area of pad design and layout such as the pad placement scheme, routing from bond pad to I/O circuitry or to power and ground rings, and the influence of such routing on the functionality and performance of the I/O circuitry and the ESD performance.

A test chip that incorporates suitable test structures to address the technical obstacles was designed and fabricated in the HP CMOS14TB process. The chips were packaged and tested to verify the viability of the approach. The verification exercise was performed for the case of 88.9-micrometer effective pitch for a 208-pin PQFP. A paper study was also done for the extension to 70- and 50-micrometer effective pitches. The results of this study will be summarized here.

Bond Pad Arrangement

In a radially staggered bond pad arrangement, every other pad is moved inward in the radial direction to form the second tier, as shown in Fig. 1. The radius used is from the center of the die and is dependent on the height of the I/O circuitry and the total number of pins. The pads are placed in a single row using 88.9-micrometer pitch, and then every other pad is moved inward in the radial direction with respect to the center of the die to form the inner row of pads. In the case of a 208-pin die with an I/O height of 358.9 micrometers, the inner-row bond pad pitch is 84.25 micrometers. Depending on the total number of pad openings and the total I/O height, the inner-row bond pad pitch will vary by a small amount. In the sample bond pad connection shown in Fig. 2, the ESD circuit is placed on the opposite side of the bond pad from the I/O circuitry. The passivation openings are 90 micrometers wide and the metal overlay for the bond pad openings is 4.8 micrometers. The ESD circuitry has an 88.9-micrometer pitch and 72.5-micrometer height. The outer-row-to-inner-row spacing is 140 micrometers. The outer-row bond pad pitch is 177.8 micrometers and the inner-row bond pad pitch is 168.95 micrometers.

[†] Wire sweep problems are created when liquid resin is forced into the plastic mold cavity. Wires can be moved closer together by the resin, causing possible shorts.

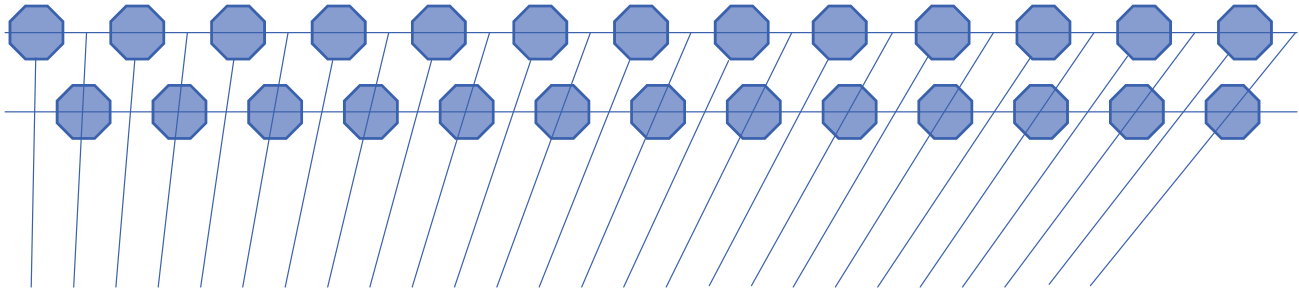


Fig. 1. Radially staggered bond pad configuration.

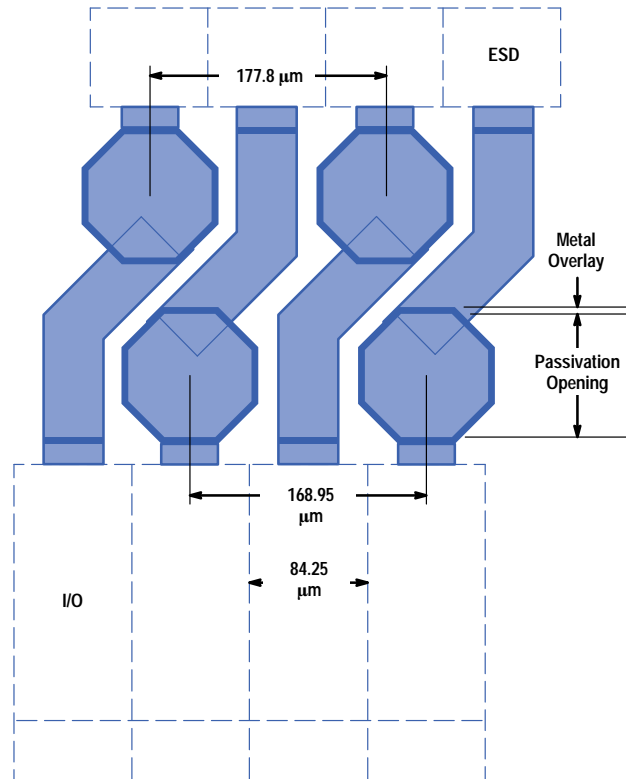


Fig. 2. Sample bond pad connection.

Square or rectangular bond pad openings with small amounts of chamfering would limit the maximum bus width for connection to bond pads. Therefore, octagonal bond pad openings with an internal radius of 90 micrometers are used. The octagonal bond pads allow wider buses for the bond pad connections to ESD and I/O circuitry. The maximum metal bus width used for the bond-pad-to-I/O or bond-pad-to-ESD connections for 208-pin die in the CMOS14TB process is 44 micrometers. The maximum interconnect metal bus width is dependent on the process design rules for passivation opening spacing to unrelated metal, minimum metal-to-metal spacing, and total number of pads. As shown in Fig. 3, the spacing between the adjacent interconnect buses gets smaller for the corner pad openings. As the number of pins increases, the inner-row pad pitch increases, while the interconnect metal spacing of the cornermost pads decreases at a faster rate. As a result, 44-micrometer metal width would be too wide in a 240-pin die. In a 100-pin or 196-pin die, the inner row pad pitches are smaller than in a 208-pin die, but because of the absence of the most extreme corner bond pads, three to six micrometer wider metal buses can be used for metal bonding pad connections to ESD or I/O circuitry.

Design Challenges

Routing and Bond Pad Placement. The longest bus connection to the outer-row bond pads from the I/O circuitry is about 197 micrometers and the shortest connection is 155 micrometers. To reduce the interconnect bus resistance to less than 0.1 ohm, all metal layers are used in parallel for the bond pad connection to the I/O or ESD circuitry.

Using the staggered bond pad configuration requires that the I/O and ESD circuitry be laid out in a narrower pitch than the existing inline configuration. It also requires special placement of bond pads and possible manual connection to bond pads. As this configuration becomes more standard, tools may be developed for automatic placement of the bond pads and

automatic bond pad interconnection to I/O and ESD circuitry. A script to perform the bond pad placement of one eighth of the chip was written in the HP ChipBuster layout editor's scripting language. However, since the available autoroute tools do not allow nonorthogonal connections, the connections to the bond pads were made manually.

Long Metal Interconnect Issues. Since all three metal layers are paralleled for the bond pad connection, the maximum interconnect bus resistance to I/O or ESD circuitry is less than 0.1 ohm for the 44-micrometer metal widths in this process. Because of this low resistance, there is no restriction on the choice of the bond pad connection location either for the supply signals or for the different I/O circuits. The 44-micrometer bus is also adequate for the voltage drops during an ESD event. Because the substrate capacitance is large compared to the mutual capacitance of the metal interconnects between neighboring signals, minimum design rules can be used for metal-to-metal spacing of the interconnecting buses without undue concern regarding cross talk.

Placing the ESD circuitry on the die boundary side of the bond pads allows a wider metal connection to the substrate ground, which has less resistance and a smaller voltage drop during an ESD event.

Latchup was found to present no problem as long as the process design guidelines were followed.

Inline versus Two-Tiered Design. In a conventional single-row inline bond pad arrangement, the minimum I/O ring size is a function of the minimum pad pitch, the I/O and ESD circuitry height including the required spacing between them, and the total pin count. The width of one side of a chip can be approximated by the following formula:

$$\text{side width} = (\text{number of pads on the side}) \times (\text{minimum I/O pitch}) + 2 \times (\text{I/O height}). \quad (1)$$

Therefore, for a 208-pin chip with 110-micrometer pad pitch when the I/O and ESD structures heights are about 500 micrometers, the minimum chip size will be $6.72 \times 6.72 \text{ mm}^2$.

In a staggered pad configuration the I/O pitch is reduced to 84.25 micrometers. Because of the two rows of bond pad openings and the narrower I/O pitch, the total block height is increased to 660 micrometers. Therefore, the minimum chip size will be about $5.70 \times 5.70 \text{ mm}^2$. This chip will be approximately 1 mm smaller on each side than a chip with an inline bond pad configuration of 110-micrometer pad pitch even though the pad height has increased by 160 micrometers.

The only differences between the inline bond pad arrangement and the staggered pad arrangement are the increase in the I/O and ESD circuitry heights, the I/O pitch, and the extra 140-micrometer height in the bonding area. Therefore, using equation 1, we can derive the following conditional expression for a square die:

$$[(\text{number of pads})/8] \times [(\text{inline I/O pitch}) - (\text{staggered I/O pitch})] < [(\text{I/O height staggered}) - (\text{I/O height inline}) + 140].$$

If this inequality is satisfied, it is a better area trade-off to use the staggered pad configuration rather than the inline bond pad placement. If the two sides of the inequality are equal, then there is no area benefit from using the staggered bond pad configuration.

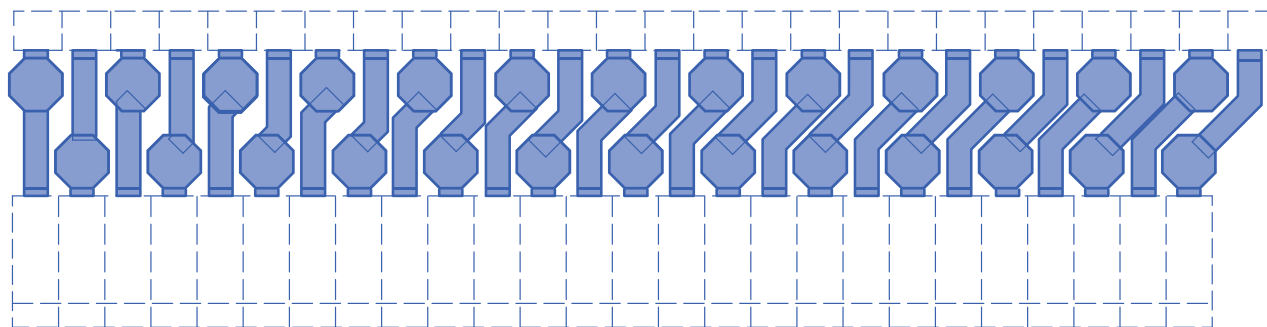


Fig. 3. One eighth of a 208-pin I/O ring.

Test Chip Architectures

Two versions of a 208-pin test die were designed and fabricated with suitable test structures. One version of the die was mainly for the reliability qualification of the package. The second version of the die was designed for verification of the functionality and performance of the I/O and ESD circuitry in the new package with the new bond pad architecture.

After considering the voltage drop because of the extra metal bus connections and the pad height, and calculating the optimal I/O pitch and optimal power and ground bus widths, the I/O and ESD circuitries were laid out in 84.25-micrometer and 88.9-micrometer pitches respectively, with small modifications from the inline I/O designs. New support pads such as corner pads and power and ground pads were designed to fit this new I/O ring structure.

As shown in Fig. 4, the bond pad placement on the two halves of each of the die sides is symmetrical around the center of each side. The bond pad placement pitch for each row is constant except in the center of each side. The two center bond pads in the outer row are placed with 110-micrometer pitch because of the minimum in-line pad pitch limitations. Effectively, the two center bond pads in the inner rows have 278.9-micrometer pitch.

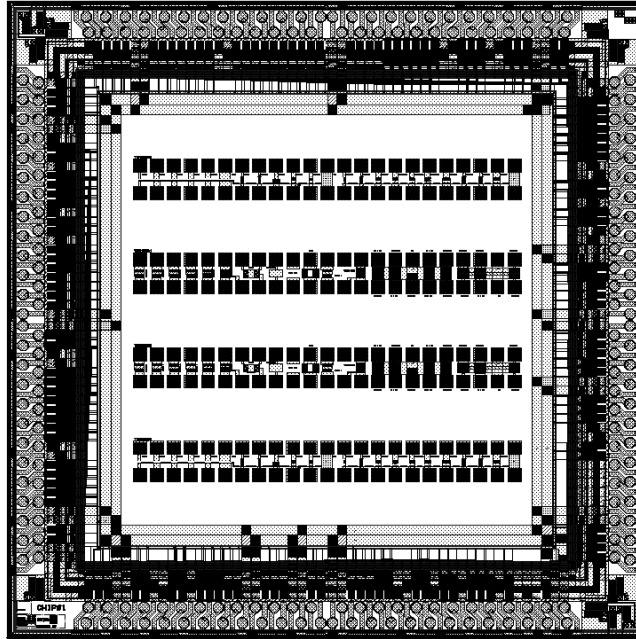


Fig. 4. Experimental chip fabricated to test the I/O and ESD performance.

The test die were fabricated and tested for package qualification and I/O and ESD performance. Over 500 parts were packaged and tested. The package qualification yield was over 98% and the parts passed 3500V HBM (human body model) ESD stress.

Extendability Study

As 90-micrometer in-line bond pad pitch with minimum passivation opening of 75 micrometers becomes feasible, the radially staggered pad pitch can be further reduced to 70-micrometer and later 50-micrometer effective pitch. These narrower pitches create a new set of issues for consideration. As the bond pad pitches are reduced, the I/O and ESD pitches are reduced as well. The finer pad pitch reduces the interconnect metal bus widths, which would result in higher bus resistance. The I/O circuitry and ESD circuitry would increase in height at a much higher rate than the 110-to-88.9-micrometer conversions, since the smaller I/O width limits the number of metal tracks that can be used for circuitry interconnects within the cell. In the case of the 100-to-84.25-micrometer I/O pitch conversion, the I/O height was only increased by about 20 micrometers. However, in the case of 70-micrometer bond pad pitch, when the I/O pitch will be about 65 micrometers, the I/O height increases from 50 to 100 micrometers depending on the different I/O functionalities. Even with this amount of height increase in I/O, the new 70-micrometer staggered pad die would be about 1 mm smaller on each side than the in-line 90-micrometer-pitch die. It can be predicted that the 50-micrometer pitch would require a much larger increase in the I/O height and may face circuit layout limitations for metal interconnect in a three-layer-metal process.

One solution to this problem would be to use processes with four or more metal layers. This will minimize the resistance in the metal interconnect buses from the bond pads to I/O or ESD circuitry, and at the same time will reduce the I/O and ESD circuitry height and possibly minimize the internal cell routing limitations that would be present in the case of 50-micrometer effective pad pitches, at the expense of a more expensive process.

Conclusion

This paper has presented a description of a new methodology for the implementation of radially staggered bonding technology from the standpoint of I/O pad circuit and ESD structure design. The algorithms by which the methodology can be implemented were presented. The issues of layout, placement, and routing for both the present design and the future migration to finer pitch were discussed.

This wire bonding solution was engineered with the goal of achieving die size reduction while minimizing the impact on cost and manufacturability. As such, it is believed that the scheme offers a significant cost reduction opportunity on pad-limited IC designs.

Acknowledgments

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