Deconstructing Queue-Based Mutual Exclusion

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We formulate a modular approach to the design and analysis of a particular class of mutual exclusion algorithms for shared memory multiprocessor systems. Specifically, we consider algorithms that organize waiting processes into a queue. Such algorithms can achieve $O(1)$ remote memory reference (RMR) complexity, which minimizes (asymptotically) the amount of traffic through the processor-memory interconnect. We first describe a generic mutual exclusion algorithm that relies on a linearizable implementation of a particular queue-like data structure that we call MutexQueue. Next, we show two implementations of MutexQueue using $O(1)$ RMRs per operation based on synchronization primitives commonly available in multiprocessors. These implementations follow closely the queuing code embedded in previously published mutual exclusion algorithms. We provide rigorous correctness proofs and RMR complexity analyses of the algorithms we present.
Deconstructing Queue-Based Mutual Exclusion

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1 Introduction

Synchronization is a fundamental challenge in asynchronous shared memory multiprocessor systems, where processes executing in parallel must exercise caution while accessing shared data structures. Unless concurrent access to such data structures is directly supported in hardware, careful coordination is necessary at the software level to prevent corruption of the data structure and ensure that processes executing on different processors reach consistent views of the data. The dominant approaches to such coordination are mutual exclusion, and non-blocking synchronization.

Mutual exclusion (ME) was formulated by Dijkstra [9], and later formalized by Lamport [17, 18]. In this approach, processes take turns accessing the shared data structure. The execution path of each process is modelled as a repeating sequence of four sections, illustrated below in Figure 1. Access to the shared data structure is confined to a special critical section (CS), to which the process must gain exclusive access by executing the entry protocol. Similarly, an exit protocol is executed upon

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<table>
<thead>
<tr>
<th>loop</th>
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<tr>
<td>Non-Critical Section (NCS)</td>
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<tr>
<td>Entry Protocol</td>
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<tr>
<td>Doorway (bounded)</td>
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<td>Waiting room</td>
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<td>Critical Section (CS)</td>
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<td>Exit Protocol</td>
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<td>forever</td>
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Figure 1: Execution path of a process participating in mutual exclusion.

completing the CS to signal that the CS can now be entered by another process. Between executions of the CS, a process lives in the *non-critical section* (NCS). The set of variables accessed by a process while in the CS or the NCS is disjoint from the set of variables accessed while in the entry or exit protocol.

An execution by a process of the entry protocol, CS and exit protocol is referred to as a *passage* (through the ME algorithm). The entry section is sometimes divided into a *doorway*, where a process enters a queue by executing a bounded number of steps, and a *waiting room*, where it waits for its predecessor in the queue to exit the CS. This type of algorithm is referred to as *first-come first-served* (FCFS). *Lockout freedom* (also referred to as *starvation freedom*) is a progress whereby every process that begins the entry protocol eventually enters the CS, provided that no process halts outside the NCS. Finally, *deadlock freedom* is a weaker property that guarantees the same but only provided that no process passes through the CS infinitely often, and is considered the weakest progress property required for correctness of a mutual exclusion algorithm.

In contrast to mutual exclusion, non-blocking synchronization requires some measure of progress regardless of the rates at which other processes are executing. For example in wait-free synchronization [13], a process must complete each access to the shared data structure in a finite number of their own steps. The key idea behind universal constructions of wait-free data structures is that faster processes assist slower ones in performing updates. To that end, processes exploit hardware synchronization primitives to agree on the order in which updates are applied, and hence on the state of the shared data.

Mutual exclusion and wait-freedom have complementary characteristics. ME is a *blocking* approach since a fast process can spend an unbounded amount of time in a busy-wait loop, which typically involves repeatedly testing or *spinning* on one variable, while waiting for another process to complete the CS and then write that variable. In contrast, in a wait-free algorithm a process ensures its own progress even if all others halt at an arbitrary point in their execution. In that sense, wait-freedom is a stronger progress property than the one underlying mutual exclusion. Not surprisingly, there exist shared object types for which wait-free implementations are provably more costly than blocking ones. For example, any wait-free *N*-process im-
Implementation of fetch-and-increment using atomic read/write registers (subsequently referred to simply as registers) and fetch-and-store requires $\Omega(\log N)$ remote memory references (RMR, discussed below) [15]. In contrast, there is a blocking implementation of fetch-and-increment from registers and fetch-and-store using only $O(1)$ RMRs. In light of its lower cost, mutual exclusion remains the dominant approach to synchronization in practice.

1.1 Time Complexity of Mutual Exclusion Algorithms

Analyzing the time complexity of ME algorithms requires some awareness of the shared memory hardware architecture as different memory operations may incur significantly different latencies. This is due to the growing disparity between processor speed and memory access speed, which motivates multiprocessor designs based on the paradigms of non-uniform memory access (NUMA) and/or caching. Two important classes of such architectures are illustrated in Figure 2 [23, 3]. In a Distributed Shared Memory (DSM) machine, each memory module can be accessed locally by some processor without involving the processor-to-memory interconnect, thus reducing much of the latency. Processors in cache-coherent (CC) machines, on the other hand, maintain local copies of data inside caches, which are synchronized by a coherence protocol. Thus, any shared memory location can become local at runtime to any processor in the CC model.

In both the DSM and CC models, memory operations are classified as either remote or local. This classification is straightforward in the DSM model as locality is determined through static allocation of a variable in particular a memory module.
In contrast, in the CC model locality of a memory operation is determined by the state of the processor’s cache, which depends on prior steps of the same processor and possibly others, as well as by the type of memory access (e.g., read versus write), which determines the behaviour of the coherence protocol. For our purposes, we consider the following ideal behaviour in the CC model: after a processor reads a variable, this variable is held in that processor’s cache and can be read locally (i.e., without incurring an RMR) until another processor writes the same variable. In both the DSM and CC models, we will assume for worst-case analysis that each process runs on a distinct processor.

Remote operations, referred to as remote memory references or RMRs, can be orders of magnitude more costly than local ones. Consequently, RMR complexity quantifies not only the overhead of accessing the processor-to-memory interconnect, but also the main source of latency incurred while executing a mutual exclusion algorithm. Mutual exclusion algorithms with bounded RMR complexity are referred to as local-spin, and have been the focus of recent research [3] on shared memory multiprocessors. In such an algorithm, all busy-waiting must be done by spinning on locally accessible variables.

To obtain a more direct measure of time complexity, one can consider the overhead of contention (for the processor-to-memory interconnect and shared memory modules) in addition to RMRs. This overhead can be quantified by counting memory stalls under the assumption that concurrent accesses to a common shared variable are serialized [10]. In that case, the $i$’th process in the serialization order incurs $i-1$ memory stalls as it waits for its predecessors to complete their operations. The exact overhead of contention depends on the shared memory architecture. Most notably, in a bus-based system a snooping protocol makes it possible for multiple processes to read a common shared variable simultaneously. In that case one counts memory stalls for concurrent writes but not for concurrent reads.

Time complexity measures for mutual exclusion algorithms typically omit local memory operations. Although local operations do have an impact on the overall latency, such a complexity measure is generally unbounded. Even if the CS is empty, due to the assumption of asynchrony there is no bound on the time that a process leaving the CS takes to execute the exit protocol and allow the next process to proceed into the CS. Furthermore, in an algorithm using only registers, even the first process to enter the CS may perform an unbounded number of steps unless it is executing solo [1]. It is possible to circumvent this problem by defining time complexity in terms of a virtual clock that ticks once for every interval of time in which every process has been given sufficient time to perform one operation on a shared memory object. The response time of a mutual exclusion algorithm is the number of such clocks ticks from the time a process leaves the NCS to the time it enters the CS [6].

1.2 Contributions of This Paper

Consider the following simple and intuitively appealing idea for an FCFS mutual exclusion algorithm: Processes wait in a queue to enter the CS. Only the head of
the queue may enter the CS. A process leaving the NCS adds itself to the end of the queue and, if it is not the head of the queue, it waits by repeatedly reading a local spin variable. A process leaving the CS removes itself from the (head of the) queue. It then writes a shared variable to signal its successor (now the new head of the queue), perhaps after checking if such a process exists, to stop waiting and proceed into the CS.

Clearly, race conditions can arise when a process contending for entry to the CS checks whether it is the head of the queue (perhaps as it does so another process is about to enter the queue), and when a process leaving the CS checks whether there is a successor in the queue (perhaps as it does so another process is about to become its successor). Handling these race conditions properly, while relying on standard synchronization primitives and using as few RMRs as possible, is a delicate task.

Several algorithms based on the above idea have appeared in the literature [4, 12, 23, 8, 22, 24, 19]. The common simple structure underlying all these algorithms, however, is obscured by the intricate details of handling the race conditions described above. Furthermore, to our knowledge, some of these algorithms have not been proved correct.

In this paper we propose a modular approach to the design and analysis of such algorithms. We first define a queue-like shared data structure, called MutexQueue. This data structure allows a process to add itself to the end of the queue, query whether it is the head of the queue, and remove itself from the head of the queue (simultaneously determining the identity of its successor in the queue, if one exists). We then present a very simple generic queue-based mutual exclusion algorithm along the lines described above, that uses this data structure as a “black box”. We prove the correctness of this algorithm based on the abstract properties of MutexQueue. This algorithm uses only a constant number of RMRs, beyond what are needed to implement the “black box” MutexQueue, and applies only a constant number of operations on MutexQueue, per passage.

We then present two implementations of MutexQueue, both using only a constant number of RMRs for each operation in the DSM and CC models. The first uses registers and the fetch-and-increment primitive (which atomically increments a shared memory word and returns its previous value) while the second uses registers and the fetch-and-store primitive (which atomically assigns a new value to a shared memory word and returns its previous value).

The two implementations of MutexQueue are not novel: they are embedded in previously published mutual exclusion algorithms; here, we have simply recast them as implementations of the MutexQueue data structure. Specifically, the first implementation of MutexQueue is based on a mutual exclusion algorithm due to Tom Anderson [4], as subsequently modified by James Anderson and Yong-Jik Kim. The second implementation of MutexQueue is based on a mutual exclusion algorithm due to Craig [8]. To our knowledge, however, these mutual exclusion algorithms have not been proved correct.\(^1\) In this paper we give rigorous correctness proofs of

\(^1\)A variant of Craig’s algorithm [8] is proved correct in [19]. This variant is intuitively simpler, but uses an array of length \(2N\) instead of \(N + 1\) to encode the queue of processes waiting to enter the critical section.
these algorithms (as implementations of MutexQueue).

The advantage of our modular approach is that it “factorizes” the common structure of some queue-based algorithms, in the form of the generic mutual exclusion algorithm. The correctness of this common part need only be proved once. What is left in each of these algorithms, can be viewed as an implementation of the MutexQueue data structure.

Our definition of the MutexQueue also sheds light on how exactly processes coordinate access to the critical section in queue-based mutual exclusion algorithms. For example, in such algorithms a process does not enter the queue and also discover whether it became the head element in one atomic step. Rather, two atomic steps are required, and are therefore represented by distinct MutexQueue operations. In contrast, a process can exit the queue and discover its successor in one atomic step. Surprisingly, sometimes a process can also exit the queue and discover no other process, even though a successor does exist! In particular, this occurs if the successor has entered the queue but has not yet queried the head element. Thus, it is the latter step (i.e., querying the head) that makes a process “visible” to its predecessor, and not the mere act of entering the queue.

2 Related Work

The RMR complexity of mutual exclusion algorithms is a function of the number of processes, $N$. The best known upper bound on the worst-case RMR complexity per passage of algorithms based on (atomic) read/write registers only is $O(\log N)$ [25, 16]. This bound is tight [5]. The same tight bound holds for the class of mutual exclusion algorithms that in addition to registers use compare-and-swap (CAS) or load-linked/store-conditional (LL/SC) – primitives that conditionally change the value of a shared memory location [11].

Using synchronization primitives such as fetch-and-store (i.e., swap between shared memory and a private register) and fetch-and-increment, it is possible to devise mutual exclusion algorithms with worst-case RMR complexity of only $O(1)$ [4, 12, 23, 8, 22, 24, 19]. The properties of these algorithms are summarized in Table 1. All of these algorithms are based on the concept of a process queue, which determines the order in which processes enter the CS and enables efficient signaling between processes that enter the CS consecutively. Thus, in addition to mutual exclusion and lockout freedom, these algorithms also satisfy FCFS.

Many of the queue-based constant-RMR mutual exclusion algorithms cited above were presented in the context of performance studies, and lack rigorous proofs of correctness. Moreover, to our knowledge the only attempt to generalize or unify
<table>
<thead>
<tr>
<th>Publication reference</th>
<th>RMR complexity CC model</th>
<th>DSM model</th>
<th>Synchronization primitives (+ read/write registers)</th>
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<tbody>
<tr>
<td>[4]</td>
<td>$O(1)$</td>
<td>unbounded</td>
<td>Fetch-and-Increment (unbounded counter)</td>
</tr>
<tr>
<td>[12]</td>
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<td>unbounded</td>
<td>Fetch-and-Store</td>
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<tr>
<td>[23]</td>
<td>$O(1)$</td>
<td>$O(1)$</td>
<td>Fetch-and-Store + Compare-and-Swap</td>
</tr>
<tr>
<td>[8]</td>
<td>$O(1)$</td>
<td>$O(1)$</td>
<td>Fetch-and-Store</td>
</tr>
<tr>
<td>[22]</td>
<td>$O(1)$</td>
<td>unbounded</td>
<td>Fetch-and-Store + Compare-and-Clear</td>
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<tr>
<td>[24]</td>
<td>$O(1)$</td>
<td>$O(1)$</td>
<td>Fetch-and-Store</td>
</tr>
<tr>
<td>[19]</td>
<td>$O(1)$</td>
<td>$O(1)$</td>
<td>Fetch-and-Store</td>
</tr>
</tbody>
</table>

Table 1: Properties of several constant RMR mutual exclusion algorithms.

```plaintext
fetch_and_\phi(var, input)
1. \text{old := var}
2. \text{var := } \phi(\text{old, input})
3. \text{return old}
```

Figure 3: Fetch-and-\phi primitive.

these algorithms, all of which are based on the process queue concept, is the generic algorithm of Anderson and Kim [2]. This algorithm solves mutual exclusion using $O(1)$ RMRs per passage given a suitable shared-memory primitive fetch-and-\phi, which corresponds to the (atomic) execution of the pseudocode shown in Figure 3.

The fetch-and-\phi primitive can be instantiated to a variety of shared-memory primitives by choosing a suitable function $\phi$. For example, a fetch-and-store corresponds to

$$\phi(\text{old, input}) \equiv \text{input}$$

Similarly, if we use $\text{input}$ to encode a pair of values $(a, b)$, a compare-and-swap corresponds to

$$\phi(\text{old, (a, b)}) \equiv \begin{cases} 
  b & \text{if } \text{old} = a \\
  \text{old} & \text{otherwise}
\end{cases}$$

where $a$ and $b$ are the expected and target value of compare-and-swap. Thus, fetch-and-\phi generalizes various types of read-modify-write primitives, including conditionals.

Unlike its predecessors, the generic fetch-and-\phi algorithm of [2] uses two process queues instead of one, in order to cope with the generic and limited assumptions on the behaviour of the fetch-and-\phi primitive. Consequently, an additional mechanism is needed to control access to the critical section, and the algorithm loses the (FCFS) property inherent in earlier single-queue solutions.

Correctness of the generic algorithm depends on a condition on the fetch-and-\phi primitive related to its ability to return distinct values over repeated invocations. This condition is formalized in terms of a property of a primitive called rank. Intuitively, the higher the rank, the better the primitive at solving mutual exclusion
efficiently with respect to RMR complexity. A rank of $2N$ or greater is sufficient for the generic algorithm, but it is not known whether rank $\Omega(N)$ is necessary for solving mutual exclusion with $O(1)$ RMRs per passage. Examples of primitives that have rank $2N$ or more include an $r$-bounded fetch-and-increment (i.e., $\phi(\text{old}, \text{input}) = \min(r - 1, \text{old} + 1)$) for $r \geq 2N$, which has rank $r$, and fetch-and-store, which has infinite rank. Compare-and-swap as well as test-and-set can also be modeled as fetch-and-$\phi$ primitives, but both have rank only two.

Any mutual exclusion algorithm that uses only compare-and-swap and registers requires $\Omega(\log N)$ RMRs [5, 11]. In contrast, there are mutual exclusion algorithms that use only fetch-and-store and registers that require only $O(1)$ RMRs (e.g., [8]). So, from the point of view of supporting RMR-efficient implementations of mutual exclusion, fetch-and-store is more powerful than compare-and-swap. It is interesting that the opposite is the case from the point of view of supporting wait-free implementations of objects. It is well-known from Herlihy’s work that compare-and-swap and registers support wait-free implementation of any object shared by any number of processes, while there are objects shared by only three processes that cannot be implemented wait-free using only fetch-and-store and registers [13].

3 Road Map

First, we present the model of computation in Section 4. In Section 5 we present our generic formulation of the queue-based mutual exclusion algorithm, and prove its correctness properties, assuming a suitable implementation of MutexQueue, a novel queue-like data structure. Then, in Sections 6 and 7, we discuss two implementations of MutexQueue, based on the fetch-and-increment and fetch-and-store primitives, respectively. Our implementations closely follow the queuing code embedded in existing queue lock algorithms [4, 8]. We conclude in Section 8 with a discussion of the applicability of our analysis technique.
4 Model of Computation and Definitions

Our model of computation is based on [14]. A concurrent system models an asynchronous shared memory system where \( N \) processes communicate by executing operations on shared objects. Formally, a concurrent system is represented as a triple \( S = (P, V, H) \), where \( P = \{0, 1, \ldots, N - 1\} \) is a set of process identifiers, \( V \) is a set of shared objects, also referred to as variables, and \( H \) is a set of execution histories. Each process identifier corresponds to a process, which is a sequential thread of control that invokes operations on objects, one at a time, and receives corresponding responses. An object represents a data structure with a well-defined set of states and set of operations that modify the state and return responses to processes. Processes and objects can be formally modelled as input/output automata [21], but here we adopt a more informal approach.

Steps

Informally, we think of the behaviour of processes in a concurrent system \( S = (P, V, H) \) as a collection of steps. There are two categories of steps – atomic and non-atomic. In an atomic step, a process \( p \in P \) applies operation \( op \) on some object \( v \in V \) and receives the response \( ret \) of this operation. This is denoted by a tuple \( (\text{ATOM}, p, v, op, ret) \). We use atomic steps to denote operations on atomic objects, such as those provided in hardware. In a non-atomic step, a process \( p \) either invokes an operation \( op \) on some object \( v \in V \), or it receives the response \( ret \) of the last operation \( p \) invoked on \( v \). The former is called an invocation step, and is represented by a tuple \( (\text{INV}, p, v, op) \). The latter is called a response step, and is represented by a tuple \( (\text{RES}, p, v, ret) \). We use non-atomic steps (along with atomic steps) to denote operations on objects that are simulated in software from atomic objects, as explained later.

Execution Histories

An execution history, or history for short, is a sequence of steps. An execution history is generated as processes accesses objects according to the transition functions of the corresponding automata, which we will describe using pseudocode. The histories we will consider contain either only atomic steps, or a combination of atomic and non-atomic steps where each object is accessed by steps of exactly one category.

We say that \( H \) is a history of (or over) object \( v \) if every step in \( H \) accesses \( v \). A response step \( e_r = (\text{RES}, p, v, -) \) in \( H \) matches the last preceding invocation step \( e_I = (\text{INV}, p, v, -) \) in \( H \) (if one exists). An invocation step is pending in \( H \) if it is not followed by a matching response step.

An operation execution in a history \( H \in H \) is either a pair of matching invocation/response steps, or a pending invocation step. We call an operation execution complete in the former case, and pending in the latter. Two operation executions are concurrent in \( H \) unless the response of one precedes the invocation of the other in \( H \). We say that \( H \) is sequential if it contains no concurrent operation executions, and

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3Here and in the remainder of the paper, “-” denotes a wildcard value.
**Object Types and Conformity to a Type**
Every object has a *type* $\tau = (P, S, s_{init}, O, R, \delta)$ where $P$ is a set of process IDs (defined as for concurrent systems), $S$ is a set of states, $s_{init} \in S$ is the initial state, $O$ is a set of operations, $R$ is the set of operation responses, and $\delta : P \times S \times O \rightarrow S \times R$ is a (one-to-many) state transition mapping. The transition mapping $\delta$ is intended to capture the behaviour of objects of type $\tau$, in the absence of concurrency, as follows: if a process $p$ applies operation $op$ to an object of type $T$ that is in state $s$, then the object may return to $p$ the response $r$ and change its state to $s'$ if and only if $(s', r) \in \delta(p, s, op)$. A complete, sequential execution history $H$ of object $v$ of type $\tau$ induces a sequence of tuples $(p_i, op_i, r_i)$ such that in the $i$'th atomic step or operation execution in $H$ (depending on the structure of $H$), process $p_i$ applies operation $op_i$ and receives response $r_i$. We say that $v$ *conforms* to $\tau$ in $H$ if there exists a sequence $s_0, s_1, s_2, \ldots$ of states of $\tau$ such that $s_0 = s_{init}$ and for each $i \geq 1$, $(s_i, r_i) \in \delta(p_i, s_{i-1}, op_i)$.

**Algorithms**
An algorithm is a concurrent system $S = (P, V, H)$ where every history $H \in H$ contains only atomic steps over $V$. We call such a history a *one-level* history, to distinguish it from the more complex execution history of an *implementation*, defined later. The set of histories is defined informally through a pseudo-code procedure for each process as follows: For each operation that a process $p$ applies to a shared variable, $H$ records an atomic step that encodes the variable, the operation applied, and its response. Accesses to private variables correspond to state changes in the automaton for a process and are not explicitly recorded in the history. Steps of different processes can be interleaved in $H$ arbitrarily. An infinite history $H$ of an algorithm is *fair* if every process that is active in $H$ takes infinitely many steps. (We do not consider terminating algorithms in this paper.)

**Implementations**
An *implementation* describes how to simulate a *target object* of a particular *target type* using a set of *base objects* of specified types. Specifically, for each operation of the target type and each process, we define an *access procedure* that computes the response of the operation under consideration by performing operations on the base objects. An implementation is a concurrent system denoted $I = (P, V, H)$ where the set of shared objects $V$ consists of a distinguished target object, denoted $T$, and a set of base objects. Histories in $H$ contain a combination of atomic and non-atomic
steps. Every history \( H \in \mathcal{H} \) is well-formed, meaning that the following conditions hold:

- \( T \) is accessed only using non-atomic steps, and for every base object \( v \in \mathcal{V} \), \( v \) is accessed only using atomic steps.
- For every base object \( v \in \mathcal{V} \), \( v \) conforms to its type in \( H|v \).
- If \( e_I = (\text{INV}, p, T, \cdot) \) is pending in \( H \) then \( e_I \) is the last non-atomic step performed by \( p \) in \( H \).
- If \( e_R = (\text{RES}, p, T, \cdot) \) is in \( H \) then \( e_R \) matches the last invocation step of \( p \) that precedes \( e_R \) in \( H \).
- If \( e_A = (\text{ATOM}, p, \cdot, \cdot, \cdot) \) is in \( H \) then it occurs after some invocation step and before the matching response (if one exists).

We call an execution history of an implementation a two-level history since operation executions on the target object and on base objects are nested.

Histories in \( \mathcal{H} \) correspond to executions of the access procedures as follows. When a process \( p \) begins executing the access procedure for operation \( op \) on \( T \), the history records the step \((\text{INV}, p, T, op)\). As \( p \) subsequently executes the access procedure, the history records corresponding atomic steps by \( p \) on base objects. Finally, when the access procedure returns a value \( ret \), then the history records the response step \((\text{RES}, p, T, ret)\). Processes may call the access procedures arbitrarily many times and in arbitrary order. An infinite history \( H \) of an implementation is fair if every process that is active in \( H \) either takes infinitely many steps, or applies a response step as its last step in \( H \). Informally, this means that in a fair history a process may not stop executing in the middle of an access procedure.

**Linearizability**

Linearizability [14] is widely accepted as a correctness condition for concurrent objects. Informally, it states that operation executions in a history of an implementation must appear to take effect instantaneously at some point between the corresponding invocation and response steps. Formally, linearizability is defined as follows. Given a history \( H \) of an implementation, \( <_H \) is the partial order over the set of operation executions in \( H \) defined as follows: \( oe_1 <_H oe_2 \) iff the response of \( oe_1 \) occurs in \( H \) before the invocation of \( oe_2 \). Two execution histories \( G \) and \( H \) are equivalent if every process executes the same sequence of steps in both histories. Letting \( T \) denote the target object, a completion of \( H|T \) is a well-formed history \( H' \) obtained from \( H \) by either completing (with a response event) or removing every pending operation execution. \( H|T \) is linearizable with respect to type \( \tau \) if it has a completion equivalent to some complete sequential history \( \bar{H} \) over \( T \) such that \( <_H \subseteq <_R \) and where \( T \) conforms to type \( \tau \) in \( \bar{H} \). In this case we say that \( \bar{H} \) is a linearization of \( H \). We denote the set of possible linearizations of \( H \) by \( \text{Lin}(H) \). We say that an implementation \( I = (\mathcal{P}, \mathcal{V}, \mathcal{H}) \) is linearizable with respect to type \( \tau \) if for every history \( H \in \mathcal{H} \), \( H|T \) is linearizable with respect to type \( \tau \).
Additional Notation
Let $G, H$ be execution histories. If $s$ is a step, we denote by $s \in H$ that step $s$ occurs in $H$, by $\text{proc}(s)$ the process that executes $s$, and by $\text{var}(s)$ the object on which $s$ operates. We denote by $G \preceq H$ that $G$ is a prefix of $H$, and by $G \prec H$ that $G$ is a proper prefix of $H$. If $v$ is an object and $H$ is an execution history such that $H|v$ is complete and sequential, then we denote the state of $v$ at the end of $H|v$ by $v^H$.

Given execution histories (or, more generally, sequences) $H$ and $G$, let $G \circ H$ denote the concatenation of $G$ and $H$ (i.e., elements of $H$ appended to $G$). If $G$ is finite, $|G|$ denotes the length of $G$. For $0 \leq i < |G|$, $G[i]$ denotes the $i$'th step (counting from 0) of $G$. $G[i..j]$ denotes the subsequence of $G$ consisting of all $G[k]$ such that $i \leq k \leq j$. 

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5 Generic Queue-Based Algorithm

5.1 The MutexQueue Type

An $N$-process MutexQueue is a queue-like object type that stores a subset of $N$ process IDs (subsequently also referred to as processes). The state of MutexQueue is an ordered pair $(Q, V)$, where $Q$ and $V$ are a sequence and a set, respectively, of elements from $\mathcal{P}$. Informally, $Q$ represents the sequence of processes waiting to enter the critical section, and $V$ is a subset of these processes that are visible. Intuitively, a process becomes visible when it “makes itself known” to its predecessor in the queue. The initial state is $(\langle \rangle, \emptyset)$. In addition, we define a special broken state $\bot$, indicating that a process has violated the etiquette for accessing MutexQueue (explained below).

A MutexQueue supports three types of operations: \texttt{enqueue()}, \texttt{isHead()}, and \texttt{dequeue()}. Informally, \texttt{enqueue()} adds the executing process to the end of the queue and always returns the response \texttt{OK}; \texttt{isHead()} makes the executing process visible and returns \texttt{true} if and only if this process is the head of the queue; and \texttt{dequeue()} removes the executing process from the head of the queue, and returns the ID of the successor process in the queue, if it exists and is visible (or $-1$ otherwise). As mentioned earlier, processes are expected to follow a certain etiquette in accessing MutexQueue. Specifically, a process must not invoke \texttt{enqueue()} if it is already in the queue, \texttt{isHead()} if it is not in the queue or is already visible, and \texttt{dequeue()} if it is not the head of the queue or is not visible. Failure to comply with this etiquette causes the MutexQueue to enter the broken state $\bot$, and thereafter all responses are completely arbitrary. These restrictions on accessing MutexQueue make it easier to implement this object. As we will see, they are observed by our generic algorithm that uses MutexQueue to solve mutual exclusion (see Section 5.2).

Prima facie, it would seem that we can have a simpler definition of MutexQueue, and a correspondingly simpler version of the generic mutual exclusion algorithm based on MutexQueue, by combining the \texttt{enqueue()} and \texttt{isHead()} operations into a single operation that adds the ID of the executing process to the end of the queue, and returns \texttt{true} if that process is the head of the queue and \texttt{false} otherwise. Unfortunately, the resulting operation seems too strong; we were not able to find an implementation for it that uses standard synchronization primitives and incurs only a constant number of RMRs. By splitting the functionality into two separate operations, such implementations become feasible.

Formally, an $N$-process MutexQueue is specified by the tuple $(\mathcal{P}, \mathcal{O}, \mathcal{R}, \mathcal{S}, \tau)$ where

$\mathcal{P} = \{0, 1, \ldots, N-1\}$

$\mathcal{O} = \{\texttt{enqueue()}, \texttt{isHead()}, \texttt{dequeue()}\}$

$\mathcal{R} = \{\texttt{true}, \texttt{false}, -1\} \cup \{0, 1, \ldots, N-1\}$

$\mathcal{S} = \{\bot\} \cup \{(Q, V) \mid Q \text{ is a permutation of a subsequence of } \langle 0, 1, \ldots, N-1 \rangle \text{ and } p \in V \text{ only if } p \in Q\}$

and the state transition mapping $\tau$ is defined as follows:
\[ \tau(p, s, \text{enqueue}()) = \begin{cases} \{(Q \circ \langle p \rangle, V), \text{OK}\} & \text{if } s = (Q, V) \text{ and } p \notin Q \\ \{(\bot, \text{ret}) \mid \text{ret} \in \mathcal{R}\} & \text{otherwise} \end{cases} \]

\[ \tau(p, s, \text{isHead}()) = \begin{cases} \{((Q \cup \{p\}), \text{true})\} & \text{if } s = (Q, V), p \in Q, p \notin V \text{ and } Q[0] = p \\ \{((Q \cup \{p\}), \text{false})\} & \text{if } s = (Q, V), p \in Q, p \notin V \text{ and } Q[0] \neq p \\ \{(\bot, \text{ret}) \mid \text{ret} \in \mathcal{R}\} & \text{otherwise} \end{cases} \]

\[ \tau(p, s, \text{dequeue}()) = \begin{cases} \{((|Q| - 1), V \setminus \{p\}), Q[1]\}) & \text{if } s = (Q, V), p \in Q, p \in V, Q[0] = p, |Q| > 1 \text{ and } Q[1] \in V \\ \{((|Q| - 1), V \setminus \{p\}), -1\}) & \text{if } s = (Q, V), p \in Q, p \in V, Q[0] = p, |Q| = 1 \text{ or } Q[1] \notin V \\ \{(\bot, \text{ret}) \mid \text{ret} \in \mathcal{R}\} & \text{otherwise} \end{cases} \]

**Observation 5.1.** Let \( H \) be an execution history over an atomic \( N \)-process MutexQueue object \( M \) such that \( M^H = (Q, V) \neq \bot \). Then the following hold:

(a) for every process \( p \), if \( p \in V \) then \( p \in Q \)

(b) for every process \( p \), \( Q \) contains at most one instance of \( p \)

Given a state \( s = (Q, V) \) of a MutexQueue object, \( s \neq \bot \), we define the following predicates and functions.

\[
QProc(s) := \{ p \mid p \in Q \} \\
VisProc(s) := V \\
empty(s) := \begin{cases} \text{true} & \text{if } Q = \langle \rangle \\ \text{false} & \text{otherwise} \end{cases} \\
head(s) := \begin{cases} Q[0] & \text{if } |Q| \geq 1 \\ \bot & \text{otherwise} \end{cases} \\
pred(s, p) = \begin{cases} q & \text{if } \langle q, p \rangle \text{ is a subsequence of } Q \\ \bot & \text{otherwise if } Q \text{ has no such subsequence} \end{cases} \\
succ(s, p) = \begin{cases} q & \text{if } \langle p, q \rangle \text{ is a subsequence of } Q \\ \bot & \text{otherwise if } Q \text{ has no such subsequence} \end{cases}
\]

Note that for every \( p \in \mathcal{P} \), the values \( \text{pred}(s, p) \) and \( \text{succ}(s, p) \) are uniquely defined by Observation 5.1 (b). If \( p, q \in \mathcal{P} \) and \( s \) is a MutexQueue state then we use the phrases “\( s \) is empty,” “\( p \) is in the queue,” “\( p \) is the head of \( s \),” “\( p \) is visible in \( s \),” “\( p \) is the successor of \( q \) in \( s \)” and “\( p \) is the predecessor of \( q \) in \( s \)” to denote the conditions \( \text{empty}(s), p \in QProc(s), p = \text{head}(s), p \in VisProc(s), p = \text{succ}(s, q), \) and \( p = \text{pred}(s, q) \), respectively.
Shared variables:

\[ \text{Wait: array } [0..N - 1] \text{ of Boolean, initially all true} \]
\[ (\text{Wait}[p] \text{ local to } p \text{ on a DSM machine}) \]
\[ M: N\text{-process MutexQueue} \]

Private per-process variables:

\[ \text{nextHead: integer } -1..N - 1 \]

Algorithm for process \( p \):

\begin{verbatim}
loop
  NCS
  M.enqueue()
  if \neg M.isHead() then
    while Wait[p].read = true do
      end
      Wait[p].write(true)
    end
  end
  CS
  nextHead := M.dequeue()
  if nextHead \neq -1 then
    Wait[nextHead].write(false)
  end
end
forever
\end{verbatim}

Figure 4: Algorithm GQME (Generic Queue-based Mutual Exclusion) for \( N \) processes.

5.2 Generic Mutual Exclusion Algorithm

In this section we analyze the mutual exclusion algorithm shown in Figure 4. In addition to an atomic MutexQueue object, the algorithm uses an array \( \text{Wait}[0..N - 1] \) of Boolean read/write registers.

Informally, the algorithm uses the MutexQueue object \( M \) to maintain a queue of processes that are competing to enter the critical section. The \( \text{enqueue}() \) operation at line 2 constitutes the doorway, and the remaining statements leading up to the CS comprise the waiting room. In the exit protocol, spanning lines 7 to 9, a process signals its successor in \( M \) (if present and visible) to exit the waiting room and proceed to the CS.

We use syntax of the form \( V.\text{op}(\text{args}) \) in Figure 4 to indicate that process \( p \) invokes operation \( \text{op}(\text{args}) \) on the shared variable \( V \). Operations on shared registers are denoted \( \text{read} \) and \( \text{write} \).

5.2.1 Correctness Properties

Mutual Exclusion (ME): at most one process is in the CS at any time.
First-Come First-Served (FCFS): processes enter the CS in the order in which they are enqueued at line 2.

Lockout Freedom (LF): if a process leaves the NCS then it eventually enters the CS.

Bounded Exit (BE): if a process leaves the CS then it enters the NCS within a bounded number of its own steps.

5.2.2 Proof of Correctness

Let $S = (P, V, H)$ be the concurrent system corresponding to Algorithm GQME where $P = \{0, 1, \ldots, N-1\}$, $V = \{M, \text{Wait}[0], \ldots, \text{Wait}[N-1]\}$, and $H$ is the set of execution histories of Algorithm GQME. Each (concurrent) execution of Algorithm GQME is represented by a one-level history $H \in \mathcal{H}$ as follows. For each operation that a process $p$ applies to a shared variable, (e.g., $M.\text{enqueue()}$ at line 2), $H$ records an atomic step.\footnote{Note that $H$ does not record steps corresponding to the private variable $\text{nextHead}$. The value of $\text{nextHead}$ is part of the local state of a process.} The sequence of steps of each process in $H$ is determined by the pseudocode shown in Figure 4. For example, if process $p$ applies operation $\text{isHead()}$ to $M$ (see line 3) with response $\text{false}$, then the next step of $p$ in $H$ (if one exists) applies $\text{read}$ to $\text{Wait}[p]$; otherwise, the next step of $p$ in $H$ (if one exists), applies $\text{dequeue()}$ to $M$. The steps of different processes can be interleaved in $H$ in any way provided that each variable in $V$ conforms to its type in $H$.

For any history $H \in \mathcal{H}$, any process $p \in P$, and any integer $i \in \mathbb{Z}^+$, we say that $p$ is in the CS in passage $i$ at the end of $H$ if and only if $p$ performs its last step in $H$ during its $i$’th passage through Algorithm GQME, and furthermore this step is: either $\langle \text{ATOM}, p, M, \text{isHead()}, \text{true} \rangle$ (see line 3); or $\langle \text{ATOM}, p, \text{Wait}[p], \text{write(true)}, \text{OK} \rangle$ (see line 5). Similarly, we say that $p$ has completed the CS in passage $i$ at the end of $H$ if and only if $H$ contains a step $\langle \text{ATOM}, p, M, \text{dequeue}(), - \rangle$ (see line 7) performed by $p$ during passage $i$ through Algorithm GQME.

For ease of exposition, we distinguish a number of phases in which a process may be at the end of a history $H \in \mathcal{H}$. The phases are defined in Table 2 and the transitions between them are illustrated in Figure 5. Each phase is bounded by steps on shared objects.

Note that the first five phases defined in Table 2 are mutually exclusive, whereas EXIT is a sub-phase of NEAR\_NCS, and is not necessarily traversed by a process in every passage through Algorithm GQME. We will subsequently use the name of a phase as a predicate indicating that a process is in the given phase, e.g., $\text{WAIT}(p)^H = \text{true}$ iff process $p$ is in the WAIT phase at the end of a history $H \in \mathcal{H}$.\footnote{Note that $H$ does not record steps corresponding to the private variable $\text{nextHead}$. The value of $\text{nextHead}$ is part of the local state of a process.}
**Table 2: Process phase definitions.**

<table>
<thead>
<tr>
<th>Phase name</th>
<th>From operation</th>
<th>To operation</th>
<th>Notes/conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>DOORWAY</td>
<td>enqueue() at line 2</td>
<td>isHead() at line 3</td>
<td>no branch at line 3</td>
</tr>
<tr>
<td>WAIT</td>
<td>isHead() at line 3</td>
<td>write at line 5</td>
<td></td>
</tr>
<tr>
<td>DONE_WAIT</td>
<td>write at line 5</td>
<td>dequeue() at line 7</td>
<td>branch from line 3 to line 6</td>
</tr>
<tr>
<td>NO_WAIT</td>
<td>isHead() at line 3</td>
<td>dequeue() at line 7</td>
<td>via the NCS</td>
</tr>
<tr>
<td>NEAR_NCS</td>
<td>dequeue() at line 7</td>
<td>enqueue() at line 2</td>
<td></td>
</tr>
<tr>
<td>EXIT</td>
<td>dequeue() at line 7</td>
<td>write at line 9</td>
<td>no branch at line 8</td>
</tr>
</tbody>
</table>

**Figure 5: Phase transitions of process p executing Algorithm GQME.**
To prove the correctness of the algorithm we will establish the following invariant.

**Invariant 5.2.** Let \( H \in \mathcal{H} \). Define \( \text{lastPred}(H, p) \) as the last process enqueued before \( p \)'s last \&\&\( \text{enqueue}() \) operation in \( H \), or \( \perp \) if no such process exists. Then \( M^H \neq \perp \) and for every \( p \in \mathcal{P} \), the following statements hold, collectively denoted Invariant 5.2–(\( H, p \)):

(a) if \( p = \text{head}(M^H) \) then

\[
\begin{align*}
\text{NEAR}_\text{NCS}(p)^H &= \text{false} \\
\text{DOORWAY}(p)^H &\implies \text{Wait}[p]^H = \text{true} \\
\text{WAIT}(p)^H &\implies \text{Wait}[p]^H = \begin{cases} 
\text{true} & \text{if } \text{lastPred}(H, p) \neq \perp \land \\
\text{false} & \text{otherwise}
\end{cases} \text{EXIT(}\text{lastPred}(H, p))^H \\
\text{DONE}_\text{WAIT}(p)^H &\implies \text{Wait}[p]^H = \text{true} \\
\text{NO}_\text{WAIT}(p)^H &\implies \text{Wait}[p]^H = \text{true}
\end{align*}
\]

(b) if \( p \in \text{QProcs}(M^H) \land p \neq \text{head}(M^H) \) then

\[
\begin{align*}
\text{DOORWAY}(p)^H &= \begin{cases} 
\text{true} & \text{if } p \notin \text{VisProcs}(M^H) \\
\text{false} & \text{otherwise}
\end{cases} \\
\text{WAIT}(p)^H &= \begin{cases} 
\text{true} & \text{if } p \in \text{VisProcs}(M^H) \\
\text{false} & \text{otherwise}
\end{cases} \\
\text{Wait}[p]^H &= \text{true}
\end{align*}
\]

(c) if \( p \notin \text{QProcs}(M^H) \) then

\[
\begin{align*}
\text{NEAR}_\text{NCS}(p)^H &= \text{true} \\
\text{Wait}[p]^H &= \text{true}
\end{align*}
\]

**Theorem 5.3.** For any \( H \in \mathcal{H} \), Invariant 5.2 holds for \( H \).

**Proof.** We proceed by induction on \(|H|\).

**Basis:** \(|H| = 0\). In this case, \( M^H \) is the initial state \( (\langle \rangle, \emptyset) \), hence \( M^H \neq \perp \). Since \( \text{empty}(M^H) \) is true, for every \( p \in \mathcal{P} \) parts (a) and (b) of Invariant 5.2–(\( H, p \)) hold trivially (since their antecedents are false), and part (c) holds because \( \text{NEAR}_\text{NCS}(p)^H \) and \( \text{Wait}[p]^H = \text{true} \) by initialization.

**Induction Hypothesis:** For any \( k > 0 \), assume Theorem 5.3 holds for all histories \( H \in \mathcal{H} \) such that \(|H| < k\).

**Induction Step:** We must prove Theorem 5.3 for all \( H \) such that \(|H| = k\). Let \( \sigma \) be the last step in \( H \) and let \( G \) satisfy \( H = G \circ \sigma \). By the IH, \( M^G \neq \perp \) and Invariant 5.2–(\( G, p \)) holds for all \( p \). Define a critical operation as a write operation
to an element of Wait or any operation on M (i.e., an operation causing a process to change phases). If \( \sigma \) is not critical, the fact that Theorem 5.3 holds for \( G \) immediately implies that it also holds for \( H \). Consequently, it suffices to prove that Theorem 5.3 holds for \( H \) if \( \sigma \) is a critical step. We proceed by cases on \( \sigma \).

**Case A:** step \( \sigma \) is an \texttt{M.enqueue()} by \( p \) (see line 2). In this case, \( p \) goes from \texttt{NEAR.NCS} to \texttt{DOORWAY}. Since \( M^G \neq \bot \) by the IH and \texttt{NEAR.NCS}(p)\textsuperscript{G}, Invariant 5.2–(G, p) implies \( p \notin QProcs(M^G) \), and \( M^H \neq \bot \) holds by the state transition relation of MutexQueue. Next, note that for every \( q \in \mathcal{P} \setminus \{p\} \), Invariant 5.2–(G, q) implies Invariant 5.2–(H, q). It remains to show Invariant 5.2–(H, p).

**Subcase A1:** \( p = head(M^H) \). Since \texttt{NEAR.NCS}(p)\textsuperscript{G}, Invariant 5.2–(G, p) implies that \( Wait[p]^G = true \). Thus, \( Wait[p]^H = true \), and part (a) of Invariant 5.2–(H, p) holds. Parts (b) and (c) follow trivially since \( p = head(M^H) \).

**Subcase A2:** \( p \neq head(M^H) \). We have \( Wait[p]^G = true \) as in subcase A1. Since \( p \notin VisProcs(M^H) \) by \( \sigma \), part (b) of Invariant 5.2–(H, p) holds. Parts (a) and (c) follow trivially since \( p \in QProcs(M^H) \) and \( p \neq head(M^H) \).

**Case B:** step \( \sigma \) is an \texttt{M.isHead()} by \( p \), with response \( ret \) (see line 3). In this case, \( p \) goes from \texttt{DOORWAY} to \texttt{WAIT} or \texttt{NO.WAIT}. Since \texttt{DOORWAY}(p)\textsuperscript{G}, Invariant 5.2–(G, p) implies \( p \in QProcs(M^G) \). Moreover, since \( M^G \neq \bot \) by the IH and \( G[M]p \) ends with an \texttt{enqueue()} step, it follows that \( p \notin VisProcs(M^G) \) and \( M^H \neq \bot \). Furthermore, \( ret \) is either \texttt{true} or \texttt{false} by the specification of MutexQueue. As in Case A, Invariant 5.2–(H, q) holds for every \( q \in \mathcal{P} \setminus \{p\} \) and it remains to show Invariant 5.2–(H, p).

**Subcase B1:** the last step in \( H \) (an \texttt{M.isHead()} returns \texttt{true}). Then \( p = head(M^H) \) by the specification of MutexQueue (since \( M^G \neq \bot \) and \texttt{NO.WAIT}(p)\textsuperscript{H} is true by the algorithm. From Invariant 5.2–(G, p) part (a) we have that \( Wait[p]^G = true \), hence \( Wait[p]^H = true \). Thus, part (a) of Invariant 5.2–(H, p) holds. Parts (b) and (c) hold trivially since \( p = head(M^H) \).

**Subcase B2:** the last step in \( H \) (an \texttt{M.isHead()} returns \texttt{false}). Then \( p \neq head(M^H) \) and \( p \in VisProcs(M^H) \) by the specification of MutexQueue (since \( M^G \neq \bot \) and \texttt{WAIT}(p)\textsuperscript{H} is true by the algorithm. We have \( Wait[p]^H = true \) as in subcase B1; since \( p \in VisProcs(M^H) \), part (b) of Invariant 5.2–(H, p) holds. Parts (a) and (c) hold trivially since \( p \neq head(M^H) \) and \( p \in VisProcs(M^H) \).

**Case C:** step \( \sigma \) is a write of \texttt{true} by \( p \) to \texttt{Wait[p]} (see line 5). In this case, \( p \) goes from \texttt{WAIT} to \texttt{DONE.WAIT}. It follows that \( M^H \neq \bot \) since \( M^H = M^G \) and \( M^G \neq \bot \) by the IH. As in the previous case, for all \( q \in \mathcal{P} \setminus \{p\} \), Invariant 5.2–(G, q) immediately implies that Invariant 5.2–(H, q) holds, and so it remains to show that Invariant 5.2–(H, p) holds. Since \texttt{WAIT}(p)\textsuperscript{G}, part (c) of Invariant 5.2–(G, p) implies that \( p \in QProcs(M^G) \). Moreover, \( Wait[p]^G = false \) by the algorithm since \( p \)'s last read of \texttt{Wait[p]} in \( G \) returns \texttt{false} and the value of \texttt{Wait[p]} is not changed until \( \sigma \) occurs. Since \( Wait[p]^G = false \), Invariant 5.2–(G, p) implies \( p = head(M^G) \). Thus, \( p = head(M^H) \) holds; furthermore, \( Wait[p]^H = true \) by the effect of the step \( \sigma \). This implies part (a) of Invariant 5.2–(H, p). Parts (b) and (c) hold trivially since \( p = head(M^H) \).
Case D: step $\sigma$ is an $M$.\texttt{enqueue}() by $p$, with response $\text{ret}$ (see line 7). In this case, $p$ goes from NO\_WAIT or DONE\_WAIT to NEAR\_NCS. Since either NO\_WAIT($p$) or DONE\_WAIT($p$), Invariant 5.2–($G, p$) implies that $p = head(M^G)$. Moreover, since $G|M|p$ ends with an $\texttt{if} \texttt{head}()$ step, and since $M^G \neq \bot$ by the IH, $\text{ret}$ is either $-1$ or $\text{succ}(M^G, p)$ by the specification of MutexQueue, and $p \in \text{VisProcs}(M^G)$. Thus, $M^H \neq \bot$ is true. Now, let $s = \text{succ}(M^G, p)$, and note that either $s = \bot$ and $\text{empty}(M^H)$, or $s = head(M^H)$. It follows that for every $q \in P \setminus \{p, s\}$, Invariant 5.2–($G, q$) implies Invariant 5.2–($H, q$). Next, consider Invariant 5.2–($H, p$). To that end, we have $p \notin QProcs(M^H)$ by the specification of MutexQueue, and $\text{Wait}[p]^G = \text{true}$ by part (a) of Invariant 5.2–($G, p$) (since $p = head(M^G)$, as argued above). Consequently, part (c) of Invariant 5.2–($H, p$) holds, and parts (a) and (b) follow trivially. Finally, we must show Invariant 5.2–($H, s$) supposing that $s \neq \bot$. Observe that $s \neq \bot$ implies $\neg \text{empty}(M^H)$ and $s = head(M^H)$ by $\sigma$. Moreover, $p \neq s$ by Observation 5.1 (b) applied to $G$, so $s \neq head(M^G)$.

Subcase D1: step $\sigma$ (an $M$.\texttt{enqueue}()) returns $-1$. It follows that $s \notin \text{VisProcs}(M^H)$. Consequently, by part(b) of Invariant 5.2–($G, s$) we have DOORWAY($s$)$^G$ and Wait[$s$]$^G = \text{true}$. Thus, DOORWAY($s$)$^H$ and Wait[$s$]$^H = \text{true}$ hold, which implies part(a) of Invariant 5.2–($H, s$). In addition, parts (b) and (c) hold trivially.

Subcase D2: step $\sigma$ (an $M$.\texttt{enqueue}()) returns a process ID $\text{ret}$. It follows that $\text{ret} = s$ and $s \in \text{VisProcs}(M^H)$. Consequently, by part (b) of Invariant 5.2–($G, s$) we have WAIT($s$)$^G$ and Wait[$s$]$^G = \text{true}$. Thus, WAIT($s$)$^H$ and Wait[$s$]$^H = \text{true}$. Observe that EXIT($p$)$^H$ holds by the algorithm, so part (a) of Invariant 5.2–($H, s$) holds. In addition, parts (b) and (c) hold trivially.

Case E: step $\sigma$ is a write of $\texttt{false}$ by $p$ to $\text{Wait}[i]$ for some $i$ (see line 9). In this case, $p$ leaves EXIT (which is part of NEAR\_NCS) and remains in NEAR\_NCS. As in Case C, it follows that $M^H \neq \bot$. Let $D$ and $E$ be prefixes of $G$ such that $E = D \circ \langle \text{ATOM}, p, M, \text{\texttt{enqueue}}(i), i \rangle$ and $|D|$ is maximal. Since $M^G \neq \bot$ it follows that $M^D \neq \bot$, $M^E \neq \bot$, $p \in QProcs(M^D)$, and $p = head(M^D)$. Let $s = \text{succ}(M^D, p)$, and observe that, as in Case D, $p \neq s$, hence $s \neq head(M^D)$. Also note that $i \neq -1$ since $p$ has branched to line 9, hence $i = s$, $s \in \text{VisProcs}(M^D)$, $s \in \text{VisProcs}(M^E)$, and $s = head(M^E)$. Since, $s \neq head(M^D)$ and $s \in \text{VisProcs}(M^E)$, part (b) of Invariant 5.2–($D, s$) implies WAIT($s$)$^D$ and Wait[$s$]$^D = \text{true}$. Next, note that $p = last\text{Pred}(E, s)$ and that $p$ performs no critical steps in $G$ after $E$. Moreover, for every history $F$ such that $E \preceq F \preceq G$, EXIT($p$)$^F$ holds and so a straightforward induction on $|F|$ shows (using part (a) of Invariant 5.2–($F, s$)) that $s = head(M^E)$, Wait[$s$]$^F = \text{true}$, WAIT($s$)$^F$, and $p = last\text{Pred}(F, s)$. Thus, $s = head(M^H)$, WAIT($s$)$^H$, and $p = last\text{Pred}(H, s)$ all hold, and Wait[$s$]$^H = \texttt{false}$ by the effect of step $\sigma$. Since $\neg$EXIT($p$)$^H$, part (a) of Invariant 5.2–($H, s$) is satisfied. In addition, parts (b) and (c) hold trivially. Finally, for every $q \in P \setminus \{s\}$, note that Invariant 5.2–($H, q$) follows immediately from Invariant 5.2–($G, q$).

Lemma 5.4. Let $H \in \mathcal{H}$ and suppose that in $H$ process $p$ executes $M$.\texttt{enqueue}() in passage $i$ before $q$ executes $M$.\texttt{enqueue}() in passage $j$, and at the end of which $q$ is in the CS in passage $j$. Then $p$ has executed $M$.\texttt{enqueue}() in passage $i$ in $H$.  

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Proof. Let $H$, $p$ and $q$ be as in the hypothesis of the lemma and suppose for contradiction that $p$ has not executed $M$.dequeue() in passage $i$ in $H$. From Theorem 5.3 and Invariant 5.2–$(H, q)$, it follows that $M^H \neq \bot$ and $q = head(M^H)$. Since $p$ was enqueued in passage $i$ before $q$ in passage $j$, this implies that $p$ in passage $i$ has been dequeued in $H$. Since $M^H \neq \bot$, it follows that $p$ has executed $M$.dequeue() in passage $i$ in $H$, which contradicts the original hypothesis. \qed

Corollary 5.5. Algorithm GQME satisfies Mutual Exclusion.

Proof. Suppose for contradiction that there exists an execution history $H \in \mathcal{H}$ at the end of which distinct processes $p$ and $q$ are both in the CS, in passages $i$ and $j$, respectively. Let $\bar{H} \in Lin(H)$. Without loss of generality, suppose that in $\bar{H}$, $p$ executes $M$.enqueue() in passage $i$ before $q$ executes $M$.enqueue() in passage $j$. Note that at the end of $\bar{H}$, $p$ and $q$ are both in the CS, in passages $i$ and $j$, respectively, and in particular $p$ has not executed $M$.dequeue() in passage $i$ (since $p$ has not invoked $M$.dequeue() in passage $i$ in $H$). Thus, $\bar{H}$, $p$, and $q$ contradict Lemma 5.4. \qed
Corollary 5.6. Algorithm GQME satisfies First-Come First-Served.

Proof. Suppose for contradiction that there exists an execution history $H \in \mathcal{H}$ in which process $p$ completes its execution of $M\text{-enqueue()}$ in passage $i$ before $q$ begins its execution of $M\text{-enqueue()}$ in passage $j$, and at the end of which $q$ is in the CS in passage $j$ but $p$ has not completed the CS in passage $i$. In particular, $p$ has not invoked $M\text{-dequeue()}$ in passage $i$ in $H$. Let $\bar{H} \in \text{Lin}(H)$. Then $p$ executes $M\text{-enqueue()}$ in passage $i$ before $q$ executes $M\text{-enqueue()}$ in passage $j$ in $\bar{H}$. Furthermore, at the end of $H$, $q$ is in the CS in passage $j$ but $p$ has not executed $M\text{-dequeue()}$ in passage $i$ (since $p$ has not invoked $M\text{-dequeue()}$ in passage $i$ in $H$). Thus, $H$, $p$, and $q$ contradict Lemma 5.4.

Theorem 5.7. Algorithm GQME satisfies Lockout Freedom.

Proof. Suppose for contradiction that there is an infinite fair history $H \in \mathcal{H}$ in which some process $p$ begins some passage $i$ and then takes infinitely many steps but never completes passage $i$. By the structure of the algorithm, $p$ in passage $i$ loops forever at line 4, repeatedly reading $\text{Wait}[p] = \text{true}$. Let $E$ be a prefix of $H$ up to but not including the last step $(\text{ATOM}, p, M, \text{enqueue()}, \text{OK})$ (see line 2). Choose $p$ so that $|E|$ is minimal. Let $F$ be a prefix of $H$ up to and including the last step $\langle \text{ATOM}, p, M, \text{isHead()}, \text{ret} \rangle$ for some response ret. Since $p$ loops forever at line 4 it follows that $F$ exists, $E \preceq F$, and $\text{ret} = \text{false}$. Furthermore, $M^F \neq \perp$ by Theorem 5.3, and $p \neq \text{head}(M^F)$ since $\text{ret} = \text{false}$, so $\text{pred}(M^F, p) \neq \perp$. Let $q = \text{pred}(M^F, p)$ and note that since $|E|$ minimal and since $H$ is fair, $q$ eventually enters phase NEAR_NCS in $H$ after $F$. In particular, $q$ eventually executes $(\text{ATOM}, q, M, \text{dequeue}(), p)$, $(\text{ATOM}, q, \text{Wait}[p], \text{write}(\text{false}), \text{OK})$, in that order, corresponding to line 7 and line 9. Now let $G$ be any prefix of $H$ such that $F \preceq G \preceq H$, in which $q$ has executed the above two steps. It follows that $\text{Wait}[p]^G = \text{false}$, which contradicts $p$ repeatedly reading $\text{Wait}[p] = \text{true}$ at line 4 in $H$ after the prefix $F$. (We do not consider the possibility of $p$ looping forever during a $\text{dequeue()}$ operation on $M$ because we assume in this section that $M$ is an atomic base object. Later on we will show for each implementation of MutexQueue that each operation on the implemented object incurs $O(1)$ steps.)

Theorem 5.8. Algorithm GQME satisfies the bounded exit property.

Proof. The result follows directly from the structure of Algorithm GQME. (We do not consider the number of steps incurred during a $\text{dequeue()}$ operation on $M$ because we assume in this section that $M$ is an atomic base object. Later on we will show for each implementation of MutexQueue that a call to $\text{dequeue()}$ incurs $O(1)$ steps.)

Theorem 5.9. Algorithm GQME has RMR complexity $O(1)$ per passage in both the CC and DSM models provided that each operation on $M$ incurs $O(1)$ RMRs.
Proof. Note that each passage involves only three MutexQueue operations, at most two atomic write operations, and an unbounded number of atomic read operations at line 4. So, it suffices to show that a process performs $O(1)$ remote memory references at line 4. This is obvious in the DSM model since $\text{Wait}[p]$ is local to $p$, in which case a process incurs zero RMRs on line 4. Now consider the CC model. Note that $p$ incurs at most one RMR at line 4 before $\text{Wait}[p] = \text{true}$ is local to $p$ (if this ever occurs). Also, $p$ is the only process that can assign $\text{Wait}[p] = \text{true}$, so a subsequent cache miss implies that $p$ reads $\text{Wait}[p] = \text{false}$. Thus, $p$ breaks out of the busy-wait loop at line 4 after at most two RMRs in total.

6 Wait-free Implementation of MutexQueue Using Fetch-and-Increment

The implementation of an $N$-process MutexQueue object described in Figure 6 is based on the mutual exclusion algorithm of T. Anderson [4], as modified by J. Anderson and Y.-J. Kim for efficient operation in the DSM model (see footnote 7 in [2]). It relies on a shared object supporting a fetch-and-increment ($\text{F&I()}$) operation, which atomically increments a variable and returns its previous value. We assume that this shared object can also be reset to an initial value, e.g., via a write.

Implementation MQFI (Figure 6) explicitly maintains a queue of processes using a pair of circular arrays. When a process enqueues itself, it obtains an index in the two arrays by atomically incrementing variable $\text{Ctr}$ at line 1. Thus, the set of processes enqueued at a given time maps to a contiguous (modulo $N$) block of array indices. The array $\text{Proc}$ stores the IDs of enqueued processes (that are visible), and array $\text{Stat}$ tracks the index of the head element and the visibility of each process. Roughly speaking, this is done as follows: when a process $p$ enqueues itself after a predecessor $q$, it is assigned array index $i$, where $\text{Stat}[i] = 0$. This value of $\text{Stat}[i]$ indicates that $p$ is neither visible nor the head of the MutexQueue. $\text{Stat}[i]$ later becomes 1 if either $p$ becomes visible or $q$ dequeues itself, making $p$ the head element. $\text{Stat}[i]$ becomes 2 once both $p$ has become visible and $q$ has dequeued itself. Finally, $\text{Stat}[i]$ is reset back to 0 when $p$ dequeues itself. Elements of $\text{Stat}$ are updated atomically using fetch-and-increment to ensure that processes performing concurrent $\text{isHead()}$ and $\text{dequeue()}$ operations receive consistent views of the MutexQueue object (recall the discussion of race conditions in the second paragraph of Section 1.2).
Shared variables:

- **Stat**: array [0..N − 1] of integer 0..2
  - initially $Stat[i] = \begin{cases} 1 & \text{if } i = 0 \\ 0 & \text{otherwise} \end{cases}$
- **Proc**: array [0..N − 1] of integer 0..N − 1, uninitialized
- **Ctr**: integer, initially zero

Static private (per-process) variables:

- **index**: integer 0..N − 1, uninitialized

Procedure for operation **enqueue**() by process $p$:

1. $index := Ctr.F&I() \mod N$
2. return **OK**

Procedure for operation **isHead**() by process $p$:

3. $Proc[index].write(p)$
4. return $Stat[index].F&I() = 1$

Procedure for operation **dequeue**() by process $p$:

5. $Stat[index].write(0)$
6. if $Stat[(index + 1) \mod N].F&I() = 1$ then
7. return $Proc[(index + 1) \mod N].read()$
8. else
9. return $-1$
end

Figure 6: Implementation MQFI ($N$-process MutexQueue implementation using Fetch-and-Increment).
6.1 Proof of Correctness

We denote Implementation MQFI (shown in Figure 6) of type MutexQueue formally as $I_{MQFI} = (\mathcal{P}, \mathcal{V}, \mathcal{H})$ where $\mathcal{P} = \{0..N - 1\}$ and $\mathcal{V}$ consists of: the base objects $\{Ctr, Stat[0..N - 1], Proc[0..N - 1]\}$, denoted subsequently as the set $\mathcal{B}$, and a target object $M$. Each $H \in \mathcal{H}$ is a two-level execution history where processes call the procedures $enqueue()$, $isHead()$ and $dequeue()$ as explained in Section 4. For each such procedure call, $H$ records an invocation step on $M$ for the corresponding operation and, if the procedure call terminates, a matching response step on $M$ with a response equal to the value returned by the procedure call. Similarly, $H$ contains an atomic step for each operation that a process applies to one of the base objects $\mathcal{B}$.

Implementation $I_{MQFI}$ simulates a MutexQueue object that can be used in Algorithm GQME (Figure 4) provided that it is linearizable with respect to the MutexQueue type, and that each call to an access procedure incurs $O(1)$ steps. The latter property follows easily from the structure of the access procedures and also implies $O(1)$ RMR complexity. Therefore, we focus at linearizability. Specifically, we must show that for every $H \in \mathcal{H}$, $H|M$ is linearizable with respect to the MutexQueue type. To that end, we will explicitly construct a candidate linearization $\bar{H}$ of $H|M$, and prove that $M$ conforms to the MutexQueue type. We will do this using an invariant that relates the state of the base objects to the “linearized state” of $M$, which is determined by our candidate linearization.

Given $H \in \mathcal{H}$, we construct $\bar{H}$ as follows. Recall that in Figure 6, the access procedure for each operation of type MutexQueue contains one or more accesses to base objects. For each MutexQueue operation execution in $H$, we define one of these base object accesses as the linearization point of that operation execution. Intuitively (and as we will prove in Theorem 6.3), the order of the linearization points determines the order in which the MutexQueue operations that contain them are linearized. Specifically, the linearization point of

- an $enqueue()$ operation execution is the base object step $Ctr.F&I()$ at line 1;
- an $isHead()$ operation execution is the base object step $Stat[index].F&I()$ at line 4;
- a $dequeue()$ operation execution in which $Stat[(index + 1) \mod N].F&I()$ at line 6 returns 1 is the base object step $Proc[(index + 1) \mod N].read()$ at line 7; and
- a $dequeue()$ operation execution in which $Stat[(index + 1) \mod N].F&I()$ at line 6 returns a value other than 1 is that base object step itself.

Note that the response of a MutexQueue operation execution is uniquely determined if its linearization point has occurred. For $enqueue()$, the response is always $OK$. For $isHead()$, the response is $true$ if and only if the linearization point’s response is 1. For $dequeue()$, the response is the response of the linearization point, if the $F&I()$ at line 6 returns 1; and $-1$, otherwise.
For any $H \in \mathcal{H}$, let $\bar{H}$ denote the complete sequential history over $M$ defined below, based on the linearization points present in $H$:

- $\bar{H}$ contains each operation execution invoked in $H|M$ whose linearization point appears in $H$, with the response determined by this linearization point, and no other steps.
- Operation executions in $\bar{H}$ occur in the same order as the corresponding linearization points in $H$.

Note that, by definition, $\bar{H}$ is a history over the target object $M$, so we can use the notation $\text{succ}(M\bar{H}, p)$ and $\text{pred}(M\bar{H}, p)$ defined in Section 5.1. We also make extensive use of the following notation: $\text{index}^H$ is the last value read from $\text{Ctr}$ by $p$ in $H$, reduced mod $N$, or $\perp$ if $H|p|\text{Ctr} = \langle \rangle$. Informally, $\text{index}^H$ denotes the value of the private variable $\text{index}_p$ at the end of $H$, assuming that $\text{index}$ is updated atomically with the response of $\text{F&I()}$ at line 1 of $\text{enqueue()}$.

**Observation 6.1.** For any $G, H \in \mathcal{H}$ such that $G \preceq H$, $\bar{G} \preceq \bar{H}$.

Informally, the following lemma says that two processes currently in the queue cannot be assigned the same array index.

**Lemma 6.2.** For any $H \in \mathcal{H}$ and for any $p, q \in P$ suppose that $\bar{H} \in \text{Lin}(H|M)$, $M\bar{H} \neq \perp$, $p \in Q\text{Proc}(M\bar{H})$, $q \in Q\text{Proc}(M\bar{H})$, and $\text{index}^H_p = \text{index}^H_q$. Then $p = q$.

**Proof.** Suppose for contradiction that $p \neq q$. Without loss of generality, assume that $p$'s last $\text{enqueue()}$ in $\bar{H}$ precedes $q$'s last $\text{enqueue()}$. Then $q$ is the $k$'th process enqueued after $p$ in $\bar{H}$ for some $k = mn$ and some $m \geq 1$. Let $(Q, V) = M\bar{H}$. It follows that $|Q| \geq k + 1$ (i.e., $Q$ contains at least $p$ and a chain of $k$ successors up to and including $q$). Since $m \geq 1$ it follows that $k + 1 > N$, so by the pigeonhole principle $Q$ contains two instances of some element, which contradicts Observation 5.1 (b).

Next, define a *bad* MutexQueue operation execution as one that violates the access etiquette for MutexQueue. More precisely, if $H \in \mathcal{H}$ then a MutexQueue operation execution $oe$ by process $p$ in $H$ is bad if and only if there exists a prefix $G$ of $H$ that contains the invocation of $oe$ but not its linearization point, such that $G \in \text{Lin}(G|M)$, $M^G \neq \perp$, and one of the following holds:

- $oe$ is $\text{enqueue()}$ and $p \in Q\text{Proc}(M^G)$
- $oe$ is $\text{isHead()}$ and either $p \notin Q\text{Proc}(M^G)$ or $p \in \text{VisProc}(M^G)$
- $oe$ is $\text{dequeue()}$ and either $p \neq \text{head}(M^G)$ or $p \notin \text{VisProc}(M^G)$

The following theorem establishes the correctness of Implementation MQFI.


**Theorem 6.3.** For any \( H \in \mathcal{H} \), \( H|M \) is linearizable with respect to type MutexQueue.

**Proof.** We will prove by induction on \(|H|\) the following claim:

If \( H \) does not contain any bad operation executions then \( \bar{H} \in \text{Lin}(H|M) \), \( M^\bar{H} \neq \perp \), and the values of the elements of \( \text{Stat} \) at the end of \( H \) are as follows:

\[
\text{Stat}[i]^H = \begin{cases} 
2 & \text{if } \exists p \in P : \text{index}_{p}^H = i \land p = \text{head}(M^\bar{H}) \land p \in \text{VisProcs}(M^\bar{H}) \land \text{in } H, p \text{ has not written Stat} \langle i \rangle \text{ at line 5 of dequeue()} \text{ since last invoking enqueue()} \\
2 & \text{if } \exists p \in P : \text{index}_{p}^H = i \land p \neq \text{head}(M^\bar{H}) \land p \in \text{VisProcs}(M^\bar{H}) \land \text{pred}(M^\bar{H}, p) \neq \perp \land \text{pred}(M^\bar{H}, p) \text{ is between lines 6 and 7 of dequeue()} \text{ in } H \\
1 & \text{if } \exists p \in P : \text{index}_{p}^H = i \land p \neq \text{head}(M^\bar{H}) \land p \in \text{VisProcs}(M^\bar{H}) \land (\text{pred}(M^\bar{H}, p) = \perp \lor \text{pred}(M^\bar{H}, p) \neq \perp \land \text{pred}(M^\bar{H}, p) \text{ is not between lines 6 and 7 of dequeue()} \text{ in } H) \\
1 & \text{if } \exists p \in P : \text{index}_{p}^H = i \land p = \text{head}(M^\bar{H}) \land p \notin \text{VisProcs}(M^\bar{H}) \\
1 & \text{if } \text{empty}(M^\bar{H}) \land i = \text{Ctr}^H \mod N \\
0 & \text{otherwise}
\end{cases}
\]

Informally, the above statement means the following. When \( p \) enqueues itself, \( \text{Stat}[\text{index}_p^H] \) is 1 if \( p \) is the head of \( M \) and 0 otherwise. \( \text{Stat}[\text{index}_p^H] \) is subsequently incremented once when \( p \) becomes visible, and once when \( p \) becomes the head (or is about the become the head and its predecessor has partially completed dequeue()).

The latter two operations may happen in either order. Finally, \( \text{Stat}[\text{index}_p^H] \) returns to 0 once \( p \) is visible, is the head of \( M \) and has begun dequeuing itself (i.e., executed line 5). Furthermore, when \( M \) is empty, \( \text{Stat}[i] = 1 \) if \( i \) is the array index that will be assigned to the next process that enqueues itself, and \( \text{Stat}[i] = 0 \) otherwise.

Note that, by Lemma 6.2, for every \( i \in [0..N-1] \), there is at most one \( p \in QProcs(M^\bar{H}) \) such that \( i = \text{index}_p^H \).

In the remainder of the proof we denote the predicate that \( \text{Stat}[i]^H \) has the value specified above by \( \beta(H, i) \).

**Basis:** \(|H| = 0\). It follows that \( H = \bar{H} = \langle \rangle \), so certainly \( \bar{H} \in \text{Lin}(H|M) \). Moreover, \( \text{empty}(M^\bar{H}) \) holds, so \( \beta(H, i) \) follows from the initialization of Implementation MQFI, for all \( i \in [0..N-1] \).

**Induction Hypothesis:** For any \( l > 0 \), assume that Theorem 6.3 holds for every \( H \) such that \(|H| < l\).

**Induction Step:** We must prove Theorem 6.3 for every \( H \) such that \(|H| = l\). Let \( G \) be a prefix of \( H \) of length \( l - 1 \). We proceed by cases on the last step \( \sigma \) in \( H \).

Cases A–G are when \( H \) ends with an atomic base object step and Case H is when \( H \) ends with a non-atomic step on the target object \( M \). In all these cases we assume
that $H$ does not contain a bad MutexQueue operation execution. Finally, Case I is when $H$ does contain a bad MutexQueue operation execution.

**Case A:** step $\sigma$ is a $\text{Ctr.\&I()}$ (see line 1 of $\text{enqueue()}$) In this case, 
$$H = G \circ ((\text{INV}, p, M, \text{enqueue}()), (\text{RES}, p, M, \text{OK}))$$
and $p \notin \text{QProcs}(M^G)$, since $H$ does not contain a bad operation execution. Then certainly $H \in \text{Lin}(H|M)$, and $M^H \neq \bot$. Furthermore, $p \notin \text{QProcs}(M^H)$, and $p \notin \text{VisProcs}(M^H)$. Next, note that $\text{Ctri} = \text{Ctri} + 1$ and $\text{Stati} = \text{Stati}$ for all $i \in [0..N - 1]$. Let $j = \text{index}_p^H$ (i.e., $j = \text{Ctri} \mod N$). It remains to show $\beta(H, i)$ for all $i \in [0..N - 1]$. For $i \neq j$ it follows from the IH that $\text{Stati}$ has the value stipulated by $\beta(H, i)$. Finally, consider $\text{Stati}$.

**Subcase A-i:** empty($M^G$). Then $p = \text{head}(M^H)$ and $p \notin \text{VisProcs}(M^H)$, so we must show that $\text{Stati} = 1$ (see fourth clause in the definition of $\text{Stati}$). But this follows from $\text{Stati} = \text{Stati}$ and $\beta(G, j)$ (fifth clause), as wanted.

**Subcase A-ii:** $\neg$empty($M^G$). Then $p \neq \text{head}(M^H)$ and $p \notin \text{VisProcs}(M^H)$, so we must show that $\text{Stati} = 0$ (see fifth clause in definition of $\text{Stati}$). By Lemma 6.2, there is no $q \in \text{QProcs}(M^G)$ such that $q \neq p$ and $\text{index}_q^H = j$, so $\text{Stati} = 0$ follows from $\text{Stati} = \text{Stati}$ and $\beta(G, j)$ (sixth clause), as wanted.

**Case B:** step $\sigma$ is a $\text{Proc[index}_p^G\text{].write(p)}$ (see line 3 of $\text{isHead()}$). In this case, 
$$H = G, \text{ so } M^H = M^G \text{ and } M^H \neq \bot \text{ since } M^G \neq \bot \text{ by the IH. Furthermore, } G|M = H|M, \text{ so } H \in \text{Lin}(H|M) \text{ since } G \in \text{Lin}(G|M) \text{ by the IH.}$$

**Case C:** step $\sigma$ is a $\text{Stati[index}_p^G\text{].F\&I()}$ with response $r$ for some $r$ (see line 4 of $\text{isHead()}$). In this case, 
$$H = G \circ ((\text{INV}, p, M, \text{isHead}()), (\text{RES}, p, M, r))$$
where $r = \text{true}$ if $r = 1$ and $r = \text{false}$ otherwise. Furthermore, $p \in \text{QProcs}(M^G)$ and $p \notin \text{VisProcs}(M^G)$ since $H$ does not contain a bad operation execution. Let $j = \text{index}_p^H$. Then by $\beta(G, j)$, $r = 1$ if $p = \text{head}(M^G)$ and $r = 0$ otherwise, so it follows that $H \in \text{Lin}(H|M)$ and $M^H \neq \bot$. Furthermore, $p \in \text{QProcs}(M^H)$ and $p \in \text{VisProcs}(M^H)$ hold. It remains to prove $\beta(H, i)$ for $i \in [0..N - 1]$. For $i \neq j$, we have $\text{Stati} = \text{Stati}$, and $\beta(G, i)$ implies $\beta(H, i)$. Finally, consider $\text{Stati}$. Note that $\text{Stati} = \text{Stati} + 1$, by the effect of the operation under consideration in this case.

**Subcase C-i:** $p = \text{head}(M^G)$. Then $p = \text{head}(M^H)$, and we must show that $\text{Stati} = 2$ since $p \in \text{VisProcs}(M^H)$ (see first clause in definition of $\text{Stati}$), i.e., we must show that $\text{Stati} = 1$. But this follows from $\beta(G, j)$ (fourth clause).

**Subcase C-ii:** $p \neq \text{head}(M^G)$. Then $p \neq \text{head}(M^H)$, and we must show that $\text{Stati} \in \{1, 2\}$ since $p \in \text{VisProcs}(M^H)$, (see second and third clause in the definition of $\text{Stati}$). Since $p \neq \text{head}(M^G)$, $p \in \text{QProcs}(M^G)$ (so $M^G$ is not empty), and $p \notin \text{VisProcs}(M^G)$, $\beta(G, j)$ implies that $\text{Stati} = 0$, hence $\text{Stati} = 1$, as wanted.

**Case D:** step $\sigma$ is a $\text{Stati[index}_p^G\text{].write(0)}$ (see line 5 of $\text{dequeue()}$). In this case, 
$$H = G; \text{ thus } H \in \text{Lin}(H|M) \text{ (since, by the IH, } G = H \text{ is a linearization of } G|M =$$
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\(H|M\), and \(M^H \neq \bot\) (since \(M^G \neq \bot\) by the IH). Furthermore, \(p \in QProcs(M^G)\), \(p \in VisProcs(M^G)\) and \(p = head(M^G)\) since \(H\) does not contain a bad operation execution, hence \(p \in QProcs(M^H)\), \(p \in VisProcs(M^H)\) and \(p = head(M^H)\). It remains to prove \(\beta(H,i)\) for all \(i \in [0..N - 1]\) Let \(j = index_p^H\) and note that for all \(i \in [0..N - 1]\), \(i \neq j\), \(\beta(H,i)\) follows directly from \(\beta(G,i)\). Finally, \(\beta(H,j)\) holds since \(p = head(M^H)\), \(p \in VisProcs(M^H)\), and \(Stat[j]^H = 0\) by the effect of step \(\sigma\). (See the sixth clause in the definition of \(Stat[j]^H\), noting that, at the end of \(H\), \(p\) has just completed line 5.)

**Case E:** step \(\sigma\) is a \(Stat[(index_p^G + 1) mod N].F&I()\) that returns \(ret \neq 1\) (see line 6 of \(dequeue()\)). In this case,

\[\bar{H} = G \circ ((INV, p, M, dequeue()), (RES, p, M, -1))\]

Since, by assumption, \(H\) contains no bad operation executions, \(p \in QProcs(M^G)\), \(p \in VisProcs(M^G)\) and \(p = head(M^G)\). By the IH, \(M^G \neq \bot\) and so \(M^H \neq \bot\). Let \(j = index_p^H\), \(k = j + 1\) mod \(N\), and \(q = succ(M^G, p)\). Thus, if \(q \neq \bot\) then \(q = head(M^H)\). Furthermore, we claim that if \(q \neq \bot\) then \(q \notin VisProcs(M^G)\). For, if not, \(\beta(G,k)\) (third clause) would imply that \(Stat[k]^G = 1\), which would contradict the hypothesis of the case – specifically that \(ret \neq 1\). Recall from the transition function of MutexQueue that a \(dequeue()\) operation applied to a state in which the head of the queue has no successor or has a successor that is not visible returns \(-1\). Thus, \(H \in Lin(H|M)\), as wanted. It remains to show that \(\beta(H,i)\) holds for all \(i = [0..N - 1]\). This follows immediately by the IH \(\beta(G,i)\) for all \(i \neq j, k\).

To see that \(\beta(H,j)\) holds, we must prove that \(Stat[j]^H = 0\). (This is because \(j = index_p^H, p \neq head(M^H)\) and \(p \notin VisProcs(M^H)\), so clause six applies in the definition of \(Stat[j]^H\). We assume here that \(N > 1\), so if \(empty(M^H)\) then \(j \neq Ctr^H\) mod \(N\) since \(k = Ctr^H\) mod \(N\) and \(j \neq k\). The case \(N = 1\) is easy to show, noting that \(j = k\).) Since \(Stat[j]^H = Stat[j]^G\), it suffices to prove that \(Stat[j]^G = 0\). Observing that \(j = index_p^G, p = head(M^G)\), \(p \in VisProcs(M^G)\) and in \(G\), \(p\) has executed line 5 of \(dequeue()\) since its last invocation of \(enqueue()\), we conclude (see clause six in the definition of \(Stat[j]^G\)) that, \(Stat[j]^G = 0\), as wanted.

Finally, to see that \(\beta(H,k)\) holds, we consider two cases.

**Subcase E-i:** \(q = \bot\). In this case, \(empty(M^H)\) and \(k = Ctr^H\) mod \(N\). Thus, we must prove that \(Stat[k]^H = 1\) (see fifth clause in the definition of \(Stat[k]^H\)). By the IH, \(Stat[k]^G = 0\) (see sixth clause in the definition of \(Stat[k]^G\)). By the effect of step \(\sigma\), \(Stat[k]^H = Stat[k]^G + 1\). Thus, \(Stat[k]^H = 1\), as wanted.

**Subcase E-ii:** \(q \neq \bot\). As argued above, in this case \(q \notin VisProcs(M^G)\), hence \(q \neq VisProcs(M^H)\). Furthermore, \(q = head(M^H)\). Thus, we must prove that \(Stat[k]^H = 1\) (see fourth clause in the definition of \(Stat[k]^H\)). We also have \(q \neq head(M^G)\) (because \(p = head(M^G)\) and \(p\)'s successor, cannot be the same as \(p\) by Observation 5.1 (b)). Thus, by the IH, \(Stat[k]^G = 0\) (see sixth clause in the definition of \(Stat[k]^G\)). By the effect of step \(\sigma\), \(Stat[k]^H = Stat[k]^G + 1\). Thus, \(Stat[k]^H = 1\), as wanted.

**Case F:** step \(\sigma\) is a \(Stat[(index_p^G + 1) mod N].F&I()\) with return value 1 (see line 6 of \(dequeue()\)). In this case, \(\bar{H} = G\); thus \(\bar{H} \in Lin(H|M)\) (since, by the IH,
\(G = H\) is a linearization of \(G|M = H|M\), and \(M^H \neq \perp\) (since \(M^G \neq \perp\) by the IH). Since \(H\) does not contain a bad operation execution, \(p \in Q\)Procs\((M^G)\), \(p \in \text{VisProcs}(M^G)\) and \(p = \text{head}(M^G)\). Let \(j = \text{index}^H \), \(k = j + 1 \mod N\), and \(q = \text{succ}(M^G, p)\). It remains to prove that \(\beta(H, i)\) holds for all \(i \in [0..N-1]\). This follows immediately by the IH \(\beta(G, i)\) for all \(i \neq j, k\). The argument proving that \(\beta(H, j)\) holds is exactly as in Case E. Finally, consider \(\beta(H, k)\). Since \(k = \text{index}^G\), \(q = \text{succ}(M^G, p), q \neq \text{head}(M^G)\) (by Observation 5.1 (b)), and \(\text{Stat}[k]^G = 1\) by the hypothesis of this case, it follows by the IH \(\beta(G, k)\) that \(q \in \text{VisProcs}(M^G)\) (see clause three of the definition of \(\text{Stat}[k]^G\)). Furthermore, since \(H\) does not contain any bad operation executions by the IH, \(q\) is not executing a pending dequeue() in \(G\), and has not yet reached line 5 since last invoking enqueue(). Thus, \(k = \text{index}^H\), \(q \in \text{VisProcs}(M^H)\), \(\text{Stat}[k]^H = \text{Stat}[k]^G + 1 = 2\) and \(q = \text{head}(M^H)\) by the effect of step \(\sigma\), so \(\beta(H, k)\) holds (see first clause in the definition of \(\text{Stat}[k]^H\)).

**Case G:** step \(\sigma\) is a Proc\([-\text{index}^G + 1 \mod N].\text{read()}\) that returns ret for some ret (see line 7 of dequeue()). In this case,

\[
\bar{H} = G \circ (⟨\text{INV}, p, M, \text{dequeue()}⟩, ⟨\text{RES}, p, M, \text{ret}⟩).
\]

Let \(j = \text{index}^H, k = j + 1 \mod N\), and \(q = \text{succ}(M^G, p)\). Note that \(p \in Q\)Procs\((M^G)\), \(p \in \text{VisProcs}(M^G)\) and \(p = \text{head}(M^G)\) as in Case E, so \(\bar{H} \in \text{Lin}(H|M)\) provided that ret = q. Also note that \(q \neq \perp\), since if \(F \leq G\) where \(F\) ends just before \(p\)'s last F&I() operation (i.e., line 6 of dequeue()) then \(\text{succ}(M^F, p) \neq \perp\) follows from the arguments in Case F, and \(\text{succ}(M^F, p) = \text{succ}(M^G, p)\). Similarly, it follows that \(q \in \text{VisProcs}(M^G)\) and that \(q\) has not begun executing dequeue() by the end of \(G\). From Lemma 6.2 and Implementation MQFI, it follows that no process has overwritten Proc\([k]\) since \(q\) last wrote it, so \(\text{Proc}[k] = q\), and ret = q, which implies that \(\bar{H} \in \text{Lin}(H|M)\), as wanted. Now, \(\beta(H, i)\) for \(i \in [0..N-1]\), \(i \neq k\) follows directly from \(\beta(G, i)\). Finally, \(\beta(G, k)\) implies that \(\text{Stat}[k]^G = 2\) since \(q \neq \text{head}(M^G)\), \(q \in \text{VisProcs}(M^G)\), and pred(\(H, q\) = \(p\) is between lines 6 and 7 at the end of \(G\) (see second clause in definition of \(\text{Stat}[k]^G\)). Since \(\text{Stat}[k]^H = \text{Stat}[k]^G = 2\), \(q = \text{head}(M^H)\), \(q \in \text{VisProcs}(M^H)\), and \(q\) has not started dequeue() by the end of \(H\), it follows that \(\beta(H, k)\) holds (see first clause in definition of \(\text{Stat}[k]^H\)).

**Case H:** step \(\sigma\) is a non-atomic step on the target object \(M\) by process \(p\).

**Subcase H-i:** \(\sigma\) is an invocation step. Then \(\bar{H} = G\) by definition since the linearization point of every MutexQueue operation occurs after the initial invocation step. Furthermore, \(G \in \text{Lin}(H|M)\) since \(G \in \text{Lin}(G|M)\) and \(H = G \circ (s_1)\) where \(s_1\) is an invocation. Thus, \(\bar{H} \in \text{Lin}(H|M)\), and \(M^H \neq \perp\) since \(M^G \neq \perp\) by the IH.

**Subcase H-ii:** \(\sigma\) is a response step. Then the linearization point of the operation execution corresponding to \(\sigma\) has occurred in \(G\), and so \(G\) contains this operation execution. Since \(G \in \text{Lin}(G|M)\) by the IH, it follows that \(G \in \text{Lin}(H|M)\) provided that \(\sigma\) and the last step in \(H|p\) have equal return values. But the latter follows from our construction of \(\bar{H}\). (Recall that for an operation execution that is pending in \(H\), if the linearization point has occurred then the operation execution is completed with a matching response step in \(H\) that returns the uniquely-determined return value of
the access procedure.) Similarly, it follows that $H = G$. Thus, $H \in Lin(H|M)$ and $M^H \neq \bot$ since $G \in Lin(G|M)$ and $M^G \neq \bot$ by the IH.

**Case I:** $H$ contains a bad MutexQueue operation. Let $F$ be the prefix of $H$ up to but not including the first invocation step $\sigma_I$ of a bad MutexQueue operation execution. By the IH, $\bar{F} \in Lin(F|M)$ and $M^{\bar{F}} \neq \bot$. To obtain a linearization of $H|M$, first let $L = G \circ (\sigma_I, \sigma_R)$ where $\sigma_R$ is a response matching $\sigma_I$, with an arbitrary return value. Since $\sigma_I$ corresponds to a bad operation execution, it follows that $L \in Lin((G \circ (\sigma_I))|M)$, and that $M^L = \bot$. Finally, form $L'$ by appending to $L$ a complete operation execution on $M$ for all remaining operation executions in $H|M$ (i.e., those that have been invoked but are not present in $L$), say in the order of their invocation steps in $H$. Once again assign the return value for each such operation execution arbitrarily. Since $M^L = \bot$, it follows that $L' \in Lin(H|M)$. □

6.1.1 RMR Complexity

Each access procedure of Implementation MQFI performs $O(1)$ steps since there are no loops. In particular, the RMR complexity of each access procedure is $O(1)$.

6.1.2 Bounded Memory Implementation

A drawback of the above implementation is that $Ctr$ grows without bound. We now discuss how to implement $Ctr$ using bounded memory. One approach, used by [3], is to atomically subtract $N$ from $Ctr$ whenever $N - 1$ is fetched from the F&I() at line 2 of enqueue(). This ensures that $Ctr$ never grows beyond $2N - 1$ (since at most $N - 1$ other processes can increment $Ctr$ before $N$ is subtracted). The drawback of this solution is that a fetch-and-add primitive is needed in addition to (or in place of) fetch-and-increment. Another solution, brought to our attention by Prasad Jayanti, is to allow $Ctr$ to overflow, provided that it returns to zero without halting the execution. In particular, if $Ctr$ is an unsigned $m$-bit integer and $N$ divides $2^m$, then it is easy to see that Implementation MQFI remains correct (i.e., the values assigned to index are as before).
7  Wait-free Implementation of MutexQueue Using Fetch-and-Store

The implementation of an $N$-process MutexQueue presented in Figure 7 is based on the mutual exclusion algorithm of Craig [8, 7], in particular a variant brought to our attention by Prasad Jayanti. It relies on a shared object supporting a fetch-and-store (F&S) operation, which atomically writes a variable and returns its previous value. Without loss of generality, we assume that such an object also supports an ordinary write operation. (One can always simulate a write by applying a F&S and ignoring the response.)

Informally, Implementation MQFS (Figure 7) works as follows. At each point in time each process $p$ “owns” exclusively an index $myIdx_p$ of array $Queue$; the index owned by $p$ changes each time the process dequeues itself (see line 10). For this reason $Queue$ has $N + 1$ entries; if a process dequeues itself at a time when all others are enqueued, it needs to acquire an index different from those owned by the other processes and from the index it previously owned.

The processes currently in the queue implicitly form a list, the first element of which is the head of the queue. The shared variable $Last$ contains the index owned by the last process in the queue. (Whenever the queue is empty, $Last$ contains an index not currently owned by any process.) When process $p$ enqueues itself it uses F&S on $Last$ to find out its predecessor’s index (which $p$ records in $prevIdx_p$) and to atomically swap its own index into $Last$ (see line 2). The use of F&S to atomically read and update $Last$ ensures the integrity of the list of processes waiting in the queue; it is not possible for two processes getting enqueued concurrently to consider the same process as their predecessor.

Recall from the specification of MutexQueue that the operation $isHead()$ has two objectives: (a) to determine whether the process $p$ executing the operation is the head of the queue, and (b) to make $p$ visible to its predecessor, thereby ensuring that when the predecessor dequeues itself, it will “wake up” $p$. In addressing the second objective we must contend with the possibility of $p$ becoming visible to its predecessor just as that predecessor is dequeuing itself. This race condition is handled by appropriate use of F&S. We now explain how the implementation of MutexQueue achieves these two objectives.

When process $p$ enqueues itself, it sets $Queue[myIdx_p] = (myIdx_p, p)$ (see line 1). When $p$ dequeues itself, it sets $Queue[myIdx_p]$ to a value different from $(myIdx_p, -)$, specifically to $(prevIdx_p, p)$ (see line 6). (We use F&S for this assignment because of the race condition mentioned above, as we will explain shortly.)

When it executes operation $isHead()$, process $p$ signals its predecessor that it has become visible by swapping the index it owns, $myIdx_p$, and its ID, into the predecessor’s position of array $Queue$, namely $Queue[prevIdx_p]$; it records the old value of $Queue[prevIdx_p]$ in $tempIdx_p$ and $tempId_p$ (see line 4). With this information, $p$ can determine if it is the head of the queue: this is the case if and only if its predecessor had dequeued itself by the time $p$ signalled that it is visible, i.e., if and

\[\text{In this context "-" denotes a wildcard value.}\]
only if \( tempIdx_p \neq prevIdx_p \) (see line 5).

Finally, we explain how a process \( p \) that is dequeuing itself ensures that it “wakes up” its successor, provided that the latter is visible. As we have seen, when \( p \) dequeues itself, it swaps \((prevIdx_p, p)\) (where \( prevIdx_p \neq myIdx_p \)) into \( Queue[myIdx_p] \), and records the old value of \( Queue[myIdx_p] \) into \( tempIdx_p \) and \( tempId_p \) (see line 6). There are two cases, depending on the value of \( tempIdx_p \).

1. Process \( p \) finds that \( tempIdx_p \neq myIdx_p \). In this case, \( p \)'s successor \( q \) must have executed line 4 and swapped \((myIdx_q, q)\) (where \( myIdx_q \neq myIdx_p \), since no two processes can own the same index at the same time) into \( Queue[prevIdx_q] \), i.e., into \( Queue[myIdx_p] \) (since \( p \) is \( q \)'s predecessor). This means that \( q \) became visible before \( p \) dequeued itself, and so \( p \) is in charge of waking up \( q \) when it is dequeued. Indeed, in this case, \( p \)'s call to \texttt{isHead()} returns \( q \)'s ID at line 8.

2. Process \( p \) finds that \( tempIdx_p = myIdx_p \). In this case, \( Queue[myIdx_p] \) has not been changed by \( p \)'s successor since the time when \( p \) enqueued itself and wrote \( myIdx_p \) into \( Queue[myIdx_p] \) (see line 1). This means that the successor of \( p \) is not yet visible and so \( p \) is not responsible for waking it up. Accordingly, in this case \( p \)'s \texttt{dequeue()} operation returns \(-1\) (see line 9).

### 7.1 Proof of Correctness

We proceed using the same approach as in Section 6. We denote Implementation MQFS (shown in Figure 7) of type MutexQueue formally as \( I_{MQFS} = (\mathcal{P}, \mathcal{V}, \mathcal{H}) \) where \( \mathcal{P} = \{0..N-1\} \) and \( \mathcal{V} \) consists of: the base objects \{Last, \( Queue[0..N-1] \} \), denoted subsequently as the set \( \mathcal{B} \), and a target object \( M \). Histories in \( \mathcal{H} \) model the execution of Implementation MQFS in a sense analogous to the one defined in Section 6.1 for Implementation MQFI. As before, it follows easily that each call to an access procedure incurs \( O(1) \) steps, and so we focus on linearizability. To that end, we define for any \( H \in \mathcal{H} \) a candidate linearization \( \bar{H} \) using the same approach as in Section 6.1. We also define bad operation executions exactly as in Section 6.1. For the candidate linearization, we define the linearization point of

- an \texttt{enqueue()} operation execution is the base object step \( \text{Last.F&S}(myIdx) \) at line 2; and
- an \texttt{isHead()} operation execution is the base object step \( \text{Queue[prevIdx].F&S} \) at line 4; and
- a \texttt{dequeue()} operation execution is the base object step \( \text{Queue[myIdx].F&S} \) at line 6.

Note that as in Section 6.1, the response of a MutexQueue operation execution is determined uniquely if its linearization point has been reached. For \texttt{enqueue()}\), the response is always \texttt{OK}. For \texttt{isHead()}\), the response is \texttt{true} if and only if the linearization point’s response is different from the value of \( prevIdx \) for the calling
Shared variables:

- **Queue**: array [0..N] of integer 0..N, initially Queue[i] ≠ i
- **Last**: integer 0..N, initially N

Static private (per-process) variables:

- **myIdx**: integer 0..N, initially p for process p
- **prevIdx**: integer 0..N, uninitialized
- **tempIdx**: integer 0..N, uninitialized
- **tempId**: integer 0..N − 1, uninitialized

Procedure for operation enqueue() by process p:

1. `Queue[myIdx].write((myIdx, p))`
2. `prevIdx := Last.FS(myIdx)`
3. return OK

Procedure for operation isHead() by process p:

4. `(tempIdx, tempId) := Queue[prevIdx].FS((myIdx, p))`
5. return `tempIdx ≠ prevIdx`

Procedure for operation dequeue() by process p:

6. `(tempIdx, tempId) := Queue[myIdx].FS((prevIdx, p))`
7. if `tempIdx ≠ myIdx` then
   8. `ret := tempId`
   else
   9. `ret := -1`
end
10. `myIdx := prevIdx`
11. return ret

Figure 7: Implementation MQFS (N-process MutexQueue implementation using Fetch-and-Store).
process. For dequeue(), the response is −1 if the F&S at line 6 returns an ordered pair of the form (myIdx, −), and is the second element in this ordered pair otherwise.

In the proof of correctness of Implementation MQFS it will be useful to refer to the values of private variables at the end of histories in $H$. Let $H \in H$ be a history such that $H \in \text{Lin}(H|M)$ and $M^H \neq \bot$. Let $v_p$ be a private variable of process $p$ (i.e., one of $myIdx_p$, $prevIdx_p$ or $tempIdx_p$). We use $v^H_p$ to denote the value of $v_p$ at the end of $H$, assuming that each assignment to a private variable of $p$ occurs at the same time as the response of the last base object step by $p$ that precedes that assignment in the execution corresponding to $H$. Below we also use the notion of bad operation executions, defined exactly as in Section 6.1.

For any $H \in H$ and $i \in [0..N]$, we say that $p$ owns $i$ at the end of $H$ if and only if $myIdx^H_p = i$.

We now state two observations in connection with the above definitions. Informally, these say that:

(a) The value of $myIdx_p$ after $p$ performs a dequeue() operation is the value of $prevIdx_p$ when $p$ performed the preceding enqueue(). Intuitively, this is because of line 10.

(b) The value of $prevIdx_p$ after $p$ has enqueued itself is the value that $myIdx_q$ had when $q$ was last in the queue, where $q$ is the processes that entered the queue just before $p$. Intuitively, this is because of line 2.

More formally, we have:

**Observation 7.1.** Let $H \in H$ be a history where $H \in \text{Lin}(H|M)$ and $M^H \neq \bot$, and let $G \leq H$ (note that $\tilde{G} \leq \tilde{H}$).

(a) Let $p$ be any process such that $p \in QProcs(M^G)$ and $p$ executes dequeue() exactly once in $H$ after $\tilde{G}$. Then $prevIdx^G_p = myIdx^H_p$.

(b) Let $p, q$ be any processes such that $q \in QProcs(M^G)$, $p \in QProcs(M^H)$, $q$ is the process that executes the last enqueue() preceding the last enqueue() of $p$ in $\tilde{H}$, and $q$ executes dequeue() at most once in $\tilde{H}$ following $\tilde{G}$. Then $myIdx^G_q = prevIdx^H_p$.

**Lemma 7.2.** Let $H \in H$ be a history where $H \in \text{Lin}(H|M)$ and $M^H \neq \bot$. Then the following statements hold:

1. $\forall x, y \in P, x \neq y \Rightarrow myIdx^H_x \neq myIdx^H_y$

2. $\forall x, y \in QProcs(M^H), x \neq y \Rightarrow prevIdx^H_x \neq prevIdx^H_y$

3. $\forall x \in P, y \in QProcs(M^H), if myIdx^H_x = prevIdx^H_y then y = succ(M^H, x)$

$^6\text{Lin}(H|M)$ is the set of linearizations of $H|M$, as defined in Section 4.
(4) \( \forall x \in QProcs(M^H), \text{myIdx}_x^H \neq \text{prevIdx}_x^H \)

Proof. We proceed by induction on \(|H|\). It suffices to prove (1)–(3) since (4) follows immediately from (3): if \( p \in QProcs(M^H) \) and \( \text{myIdx}_p^H = \text{prevIdx}_p^H \) then (3) implies that \( p = \text{succ}(M^H, p) \), which contradicts Observation 5.1.

Basis: \(|H| = 0\). It follows that \( \bar{H} = H = \langle \rangle \). By initialization, \( \text{myIdx}_p^H = p \) and \( p \notin QProcs(M^H) \) hold for every \( p \in \mathcal{P} \), and so (1)–(3) hold for \( H \).

Induction Hypothesis: For any \( l > 0 \), assume that Lemma 7.2 holds for all \( H \) such that \(|H| < l\).

Induction Step: We must prove Lemma 7.2 for every \( H \) such that \(|H| = l\). Let \( G \) be a prefix of \( H \) of length \( l - 1 \). We proceed by cases on the last step \( \sigma \) in \( H \). Since \( M^H \neq \bot \), it follows that \( M^G \neq \bot \).

Case A: \( \bar{G} = \bar{H} \) or \( \sigma \) is the linearization point of \text{isHead()} (line 4). In this case, for each \( p \in \mathcal{P} \), \( \text{myIdx}_p^G = \text{myIdx}_p^H \) and \( \text{prevIdx}_p^G = \text{prevIdx}_p^H \). Moreover, \( QProcs(M^G) = QProcs(M^H) \). Thus, the fact that the lemma holds for \( H \) follows directly from the fact that (by the IH) it holds for \( G \).

Case B: \( \sigma \) is the linearization point of \text{M.enqueue()} by process \( p \). Lemma 7.2 (1) for \( H \) follows directly from the IH since for every \( x \in \mathcal{P} \), \( \text{myIdx}_x^G = \text{myIdx}_x^H \). It remains to prove parts (2) and (3) of the lemma for \( H \).

Subcase B1: \( p = \text{head}(M^H) \). It follows that \( M^G \) is empty and \( QProcs(M^H) \) contains only \( p \), and so Lemma 7.2 (2) holds trivially for \( H \). Now let \( j = \text{prevIdx}_p^H \).

To prove part (3), it suffices to show that no process \( z \in \mathcal{P} \) owns \( j \) at the end of \( H \). Suppose for contradiction that for some \( z \in \mathcal{P} \) \( \text{myIdx}_z^H = j \). It follows that \( \bar{H} \) contains more than one \text{M.enqueue()}(\( z \)), otherwise \( j = N \) and \( \text{myIdx}_z^H = z \) where \( z \neq N \). Let \( r \) be the process that executes the last \text{enqueue()} preceding the last \text{enqueue()} of \( p \) in \( \bar{H} \). Let \( F \) be the prefix of \( H \) up to but not including the linearization point of the last \text{M.dequeue()} performed by \( r \); this is well-defined because \( M^G \) is empty. By Observation 7.1 (b) and the fact that \( j = \text{prevIdx}_p^H \), it follows that \( \text{myIdx}_r^F = j \). Also note that no process other than \( r \) applies a MutexQueue operation execution in \( \bar{G} \) after \( F \).

There are two cases, each leading to a contradiction.

- If \( z \neq r \) then \( \text{myIdx}_z^F = j \) since \( \text{myIdx}_z^H = j \) and \( z \) does not execute \text{deque()} in \( G \) after \( F \). At the same time \( \text{myIdx}_r^F = j \), as argued above. But \( \text{myIdx}_z^F = j \) and \( \text{myIdx}_r^F = j \) contradict part (1) of the IH for \( F \) since \( z \neq r \).

- If \( z = r \) then Observation 7.1 (a) and the fact that \( \text{myIdx}_z^H = j \), \( \text{prevIdx}_z^F = j \) and hence \( \text{prevIdx}_r^F = j \). At the same time, \( \text{myIdx}_r^F = j \), as argued above. Furthermore, \( r \in QProcs(M^F) \) by definition of \( r \) and \( F \). But \( \text{prevIdx}_r^F = j \), \( \text{myIdx}_r^F = j \) and \( r \in QProcs(M^F) \) contradict part (4) of the IH for \( F \).

Thus, Lemma 7.2 (3) holds for \( H \).

Subcase B2: \( p \neq \text{head}(M^H) \). Let \( r = \text{pred}(M^H, p) \) and let \( j = \text{prevIdx}_r^H \).
First, consider Lemma 7.2 (2) for $H$. For every $q \in P \setminus \{p\}$, $prevIdx_q^G = prevIdx_q^H$ and $q \in QProcs(M^G) \leftrightarrow q \in QProcs(M^H)$ hold, so it suffices to show that there is no $z \in QProcs(M^G)$ such that $prevIdx_z^G = j$. Suppose for contradiction that $prevIdx_z^G = j$ for some $z \in QProcs(M^G)$. Observe that $r \in QProcs(M^G)$ by the definition of $G$ and the hypothesis of Subcase B2, and that $succ(M^G, r) = \bot$ by the definition of $G$ and the hypothesis of Case B. Since $prevIdx_r^G = j$, it follows from the definition of $r$ and $G$ and Observation 7.1 (b) that $myIdx_r^G = j$. Since $prevIdx_z^G = j$ and $z \in QProcs(M^G)$ by assumption, part (3) of the IH for $G$ implies that $z = succ(M^G, r)$. But this contradicts the earlier observation that $succ(M^G, r) = \bot$.

Next, consider part (3) of the lemma. It suffices to show that for any $q \in P$, if $myIdx_q^H = j$ then $p = succ(M^H, q)$. By part (1) of the IH for $G$, $r$ is the only process that owns $myIdx_r^G$ at the end of $G$, and so by the hypothesis of Case B, $r$ is the only process that owns $myIdx_r^H$ at the end of $H$. By definition, $r = pred(M^H, p)$ and so $p = succ(M^H, r)$. Thus, Lemma 7.2 (3) holds for $H$.

**Case C:** $\sigma$ is the linearization point of $M.dequeue()$ by process $p$. Note that $p = head(M^G)$ since $M^H \neq \bot$. Let $j = prevIdx_p^G$.

First, consider Lemma 7.2 (1) for $H$. Note that for every $q \in P \setminus \{p\}$, $myIdx_q^G = myIdx_q^H$ holds. Furthermore, $myIdx_p^H = j$ by line 10 and Observation 7.1 (a). It suffices to show that no process owns $j$ at the end of $H$. Suppose for contradiction that $myIdx_z^H = j$ for some $z \in P \setminus \{p\}$. Then $myIdx_z^G = j$, $prevIdx_z^G = j$ and $p \in QProcs(M^G)$ all hold by definition of $G$ and the hypothesis of Case C, so by part (3) of the IH for $G$ it follows that $p = succ(M^G, z)$. But this contradicts the earlier observation that $p = head(M^G)$.

Next, consider Lemma 7.2 (2) for $H$. Note that for every $q \in P \setminus \{p\}$, $prevIdx_q^G = prevIdx_q^H$ and $q \in QProcs(M^G) \leftrightarrow q \in QProcs(M^H)$ hold. Furthermore, $p \notin QProcs(M^H)$ by the hypothesis of Case C. Thus, Lemma 7.2 (2) for $H$ follows directly from part (2) of the IH for $G$.

Finally, consider part (3). Note that for every $q \in P \setminus \{p\}$, the following all hold: $myIdx_q^G = myIdx_q^H$, $prevIdx_q^G = prevIdx_q^H$ and $q \in QProcs(M^G) \leftrightarrow q \in QProcs(M^H)$. Furthermore, $p \notin QProcs(M^H)$ by the hypothesis of Case C. Thus, by part (3) of the IH for $G$, it suffices to show that there is no $z \in QProcs(M^H)$ such that $prevIdx_z^H = myIdx_z^H$. Suppose for contradiction that $prevIdx_z^H = myIdx_z^H$ for some $z \in QProcs(M^H)$. Note that $z \neq p$ since $p \notin QProcs(M^H)$, and so by the hypothesis of Case C we further have $prevIdx_z^G = prevIdx_z^H$ (hence $prevIdx_z^G = myIdx_z^H$) and $z \in QProcs(M^G)$. At the same time, by line 10, Observation 7.1 (a) and the hypothesis of Case C, $prevIdx_p^G = myIdx_p^H$ and $p \in QProcs(M^G)$ both hold. Thus, we have shown that the following all hold: $prevIdx_z^G = myIdx_p^H$, $prevIdx_z^G = myIdx_p^H$, $z, p \in QProcs(M^G)$ and $z \neq p$. But this contradicts part (2) of the IH for $G$.

The following theorem establishes the correctness of Implementation MQFS.

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Theorem 7.3. For any $H \in \mathcal{H}$, $H|M$ is linearizable with respect to type MutexQueue.

Proof. We will prove by induction on $|H|$ the following claim:

If $H$ does not contain any bad operation executions then $\bar{H} \in \text{Lin}(H|M)$, $M^\bar{H} \neq \bot$, and the value of Queue at the end of $H$ is as follows:

For any $i \in [0..N]$, if $\exists p \in P$ such that at the end of $H$ $p$ owns index $i$, and has applied $\text{Queue}[\text{myIdx}].\text{write}$ at line 1 of $\text{enqueue}()$, but since last doing so $p$ has not applied $\text{Queue}[\text{myIdx}].\text{F&S}$ at line 6 of $\text{dequeue}()$, then (letting $s$ denote $\text{succ}(M^\bar{H}, p)$)

\[
\text{Queue}[i]^H = \begin{cases} 
(i, p) & \text{if } s \notin \text{VisProcs}(M^\bar{H}) \\
(\text{myIdx}^H_s, s) & \text{otherwise}
\end{cases}
\]

else $\text{Queue}[i]^H \neq (i, \bot)$.

In the remainder of the proof we denote by $\beta(H, i)$ the predicate that at the end of execution history $H$, $\text{Queue}[i]^H$ has the value specified above.

Basis: $f(H) = 0$. It follows that $H = \bar{H} = \langle \rangle$, so certainly $\bar{H} \in \text{Lin}(H|M)$. It remains to show $\beta(H, i)$ for $i \in [0..N]$, which in this case asserts that $\text{Queue}[i]^H \neq (i, \bot)$. But this follows from the initialization of Implementation MQFS.

Induction Hypothesis: For any $l > 0$, assume that Theorem 7.3 holds for every $H$ such that $f(H) < l$.

Induction Step: We must prove Theorem 7.3 for every $H$ such that $|H| = l$. Let $G$ be a prefix of $H$ of length $l - 1$. We proceed by cases on the last step $\sigma$ in $H$.

Cases A–E are when $H$ ends with an base object step, and Case F is when $H$ ends with a non-atomic step on the target object $M$. In all these cases we assume that $H$ does not contain a bad MutexQueue operation execution. Finally, Case G is when $H$ does contain a bad MutexQueue operation execution.

Case A: $\sigma$ is a $\text{Queue}[\text{myIdx}^G_p].\text{write}((\text{myIdx}^G_p, p))$ (see line 1 of $\text{enqueue}()$). In this case, $\bar{H} = \bar{G}$; thus $\bar{H} \in \text{Lin}(H|M)$ (since, by the IH, $\bar{G} = \bar{H}$ is a linearization of $G|M = H|M$), and $M^\bar{H} \neq \bot$ (since $M^\bar{G} \neq \bot$ by the IH).

To prove the theorem for $H$ it suffices to verify that $\beta(H, \text{myIdx}^H_p)$ holds; all other clauses either hold trivially (because their antecedents are false) or follow immediately from the IH. (Note that in this case $\text{myIdx}^H_p$ is the only position in Queue changed by $\sigma$, which does not change the linearized state of $M$.) Since $p$ has just completed line 1 at the end of $H$, $\beta(H, \text{myIdx}^H_p)$ asserts that $\text{Queue}[\text{myIdx}^H_p]^H = (\text{myIdx}^H_p, p)$, which indeed holds by the action of step $\sigma$.

Case B: $\sigma$ is a $\text{Last.F&S}$ (see line 2 of $\text{enqueue}()$) In this case,

$\bar{H} = \bar{G} \circ (\langle \text{INV}, p, M, \text{enqueue}() \rangle, (\text{RES}, p, M, \text{OK}))$

and $p \notin QProcs(M^G)$, since $H$ does not contain a bad operation execution. Then certainly $H \in \text{Lin}(H|M)$, and $M^\bar{H} \neq \bot$.

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In the case under consideration, all clauses of Theorem 7.3 for \( H \) either hold trivially (because their antecedents are false) or follow immediately from the IH.

**Case C:** \( \sigma \) is a \( \text{Queue}[\text{prevIdx}_p^G]\).F&S with response \( r \) for some \( r \) (see line 4 of \( \text{isHead()} \)). In this case,

\[
H = G \circ ((\text{INV}, p, M, \text{isHead}()), (\text{RES}, p, M, \text{ret}))
\]

where \( \text{ret} = \text{true} \) if \( r \neq (\text{prevIdx}_p^H, -) \) and \( \text{ret} = \text{false} \) otherwise. Furthermore, \( p \in \text{QProcs}(M^G) \) and \( p \notin \text{VisProcs}(M^G) \) since \( H \) does not contain a bad operation execution. To show that \( \bar{H} \in \text{Lin}(H|M) \) we must show that \( \text{ret} = \text{true} \) iff \( p = \text{head}(M^H) \). Let \( j = \text{prevIdx}_p^G \) and consider the following subcases.

**Subcase C1:** Some \( q \in \mathcal{P} \) owns \( j \) at the end of \( G \). Then \( p = \text{succ}(M^G, q) \) by Lemma 7.2 (3), and in particular \( q \in \text{QProcs}(M^G) \) by definition of \( \text{succ} \). Furthermore \( \text{Queue}[j]^G = (j, q) \) by the IH for \( G \) since \( p \notin \text{VisProcs}(M^G) \). Thus, \( r = (j, q) \) and so \( \text{ret} = \text{false} \), while \( p \neq \text{head}(M^H) \), hence \( p \neq \text{head}(M^H) \), as wanted.

To prove the theorem for \( H \) in the case under consideration, it suffices to verify that \( \beta(H, j) \) and \( \beta(H, \text{myIndex}_j^H) \) hold; all other clauses of Theorem 7.3 for \( H \) either hold trivially or follow immediately from the IH. (Note that in this case \( j \) is the only position of \( \text{Queue} \) that is changed by \( \sigma \), and \( q \) is the only process whose successor, namely \( p \), becomes visible as a result of step \( \sigma \); the linearized state of \( M \) is otherwise unchanged.) It follows by line 2 of the algorithm that \( \text{myIdx}_p^H = \text{prevIdx}_p^H \), and since \( \text{prevIdx}_p^H = \text{prevIdx}_p^G \) that \( \text{prevIdx}_p^H = j \). Thus, the conditions \( \beta(H, \text{myIdx}_j^H) \) and \( \beta(H, j) \) are equivalent. Furthermore, since \( p \in \text{VisProcs}(M^H) \) by the action of step \( \sigma \), \( \beta(H, \text{myIdx}_j^H) \) asserts that \( \text{Queue}[\text{myIdx}_j^H]^H = (\text{myIdx}_p^H, p) \). Indeed we have

\[
\begin{align*}
\text{Queue}[\text{myIdx}_j^H]^H &= \text{Queue}[\text{prevIdx}_p^H]^H \quad \text{because } \text{myIndex}_p^H = \text{prevIndex}_p^H \\
&= \text{Queue}[\text{prevIdx}_p^G]^H \quad \text{because } \text{prevIdx}_p^H = \text{prevIdx}_p^G \\
&= (\text{myIdx}_p^G, p) \quad \text{by the action of the last operation} \\
&= (\text{myIdx}_p^H, p) \quad \text{because } \text{myIdx}_p^H = \text{myIdx}_p^G
\end{align*}
\]

**Subcase C2:** No process owns \( j \) at the end of \( G \). It follows that \( p = \text{head}(M^G) \), otherwise by line 2 and the fact that \( H \) contains no bad operation executions it would be the case that \( \text{myIdx}_{\text{pred}(M^G, p)}^G = j \). Furthermore \( \text{Queue}[j]^G \neq (j, -) \) by the IH for \( G \). Thus, \( r \neq (j, -) \) and so \( \text{ret} = \text{true} \), while \( p = \text{head}(M^G) \), as wanted.

To prove the theorem for \( H \) in the case under consideration it suffices to verify that \( \beta(H, j) \) holds; all other clauses of Theorem 7.3 for \( H \) either hold trivially or follow immediately from the IH. (Note that in this subcase the fact that \( p \) becomes visible as a result of step \( \sigma \) does not affect the value of \( \text{Queue} \) at the position owned by \( p \)'s predecessor, since \( p = \text{head}(M^G) \) and so \( p \) has no predecessor.) By the hypothesis of subcase C2, no process owns \( j \) at the end of \( G \), hence no process owns \( j \) at the end of \( H \). Thus, \( \beta(H, j) \) asserts that \( \text{Queue}[j]^H \neq (j, -) \). Indeed we have

\[
\begin{align*}
\text{Queue}[j]^H &= (\text{myIdx}_p^G, p) \quad \text{by the action of } \sigma \\
&\neq (\text{prevIdx}_p^G, -) \quad \text{by Lemma 7.2 (4) for } G \\
&= (j, -)
\end{align*}
\]
Case D: $\sigma$ is a $\text{Queue}[\text{myIdx}_p^G].\text{F&S}$ with response $(\text{myIdx}_p^G, -)$ (see line 6 of $\text{dequeue}()$). In this case,

$$H = G \circ ((\text{INV}, p, M, \text{dequeue}()), (\text{RES}, p, M, -1)) \; .$$

Since, by assumption, $H \in \text{p Queue}$

Case D:

VisProcs to assignments to private variables take effect; in particular, in this case, the assignment trivially or follow immediately from the IH. (Recall our convention regarding when $\beta$ operation by $p$ myIdx relinquish ownership of $\beta$ meaning of $p$ has no predecessor in $H p$ prevIdx of $\text{Queue}$ asserts that $\text{Queue}$ myIdx $\beta$ prevIdx process owns Lemma 7.2 (1). Since no process owns prevIdx which holds by the IH, we have $M\neg \text{prevIdx}_p$ (see line 6 since it last applied $M\neg \text{write}$ at line 1. Thus, $H \in \text{Lin}(H|M)$.

To prove the theorem for $H$ in the case under consideration, it suffices to verify that $\beta(H, \text{myIdx}_p^G)$ and $\beta(H, \text{myIdx}_p^H)$ both hold; all other clauses for $H$ either hold trivially or follow immediately from the IH. (Recall our convention regarding when assignments to private variables take effect; in particular, in this case, the assignment to $\text{myIdx}_p$ at line 10 takes effect atomically with step $\sigma$. Thus, step $\sigma$ causes $p$ to relinquish ownership of $\text{myIdx}_p^G$ and acquire ownership of $\text{myIdx}_p^H$. Also, recall that $p$ has no predecessor in $M\neg G$, and so $p$ no longer being visible has no impact on the meaning of $\beta(H, i)$ for $i \neq \text{myIdx}_p^G, \text{myIdx}_p^H$.

First consider $\beta(H, \text{myIdx}_p^G)$. Notice that no process owns $\text{myIdx}_p^G$ at the end of $H$. This is because only $p$ owns $\text{myIdx}_p^G$ at the end of $G$ (by Lemma 7.2 (1)), and at the end of $H$ the process does not own a different index, namely $\text{myIdx}_p^G$ (note that $\text{myIdx}_p^G = \text{prevIdx}_p^G$ by line 10, and $\text{prevIdx}_p^G \neq \text{myIdx}_p^G$ by Lemma 7.2 (4)). Thus, $\beta(H, \text{myIdx}_p^G)$ asserts that $\text{Queue}[\text{myIdx}_p^G]^H \neq (\text{myIdx}_p^G, -)$. This is indeed true since

$$\text{Queue}[\text{myIdx}_p^G]^H = (\text{prevIdx}_p^G, -) \text{ by the action of step } \sigma$$

$$\neq (\text{myIdx}_p^G, -) \text{ by Lemma 7.2 (4) for } G$$

Next, consider $\beta(H, \text{myIdx}_p^H)$. By the hypothesis of Case D, in $H$ $p$ has applied $\text{Queue}[\text{myIdx}_p].\text{F&S}$ at line 6 since it last applied $\text{Queue}[\text{myIdx}_p].\text{write}$ at line 1. Thus, $\beta(H, \text{myIdx}_p^H)$ asserts that $\text{Queue}[\text{myIdx}_p^H]^H \neq (\text{myIdx}_p^H, -)$. We now prove that this is the case. We have that $\text{myIdx}_p^H = \text{prevIdx}_p^H$ (by line 10). Also, no process owns $\text{prevIdx}_p^G$ at the end of $G$: $p$ does not own it because it owns $\text{myIdx}_p^G$ and $\text{myIdx}_p^G \neq \text{prevIdx}_p^G$ (by Lemma 7.2 (4)); and no other process owns it because if one, say $z$, did then $p$ and $z$ would both own it at the end of $H$, contradicting Lemma 7.2 (1). Since no process owns $\text{prevIdx}_p^G$ at the end of $G$, by $\beta(G, \text{prevIdx}_p^G)$, which holds by the IH, we have $\text{Queue}[\text{prevIdx}_p^G]^G \neq (\text{prevIdx}_p^G, -)$. But then, since $\text{prevIdx}_p^G = \text{myIdx}_p^H$, and since step $\sigma$ does not change position $\text{prevIdx}_p^G$ of $\text{Queue}$ (it changes position $\text{myIdx}_p^G$, which is different from $\text{prevIdx}_p^G$ by Lemma 7.2 (4)), we have $\text{Queue}[\text{myIdx}_p^H]^H \neq \text{myIdx}_p^H$, as wanted.

Case E: $\sigma$ is a $\text{Queue}[\text{myIdx}_p^G].\text{F&S}$ with response different from $(\text{myIdx}_p^G, -)$ (see line 6 of $\text{dequeue}()$). In this case,

$$H = G \circ ((\text{INV}, p, M, \text{dequeue}()), (\text{RES}, p, M, m))$$

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where \( r = tempId_p^H \). Since, by assumption, \( H \) contains no bad operation executions, \( p \in QProcs(M^G) \), \( p \in VisProcs(M^G) \) and \( p = head(M^G) \). By the IH, \( M^G \neq \bot \) and so \( M^H \neq \bot \). By the case under consideration, \( Queue[myIdx_p^G]\) \( \neq (myIdx_p^G, -) \). By the IH, \( \beta(G, myIdx_p^G) \) holds, which implies that \( succ(M^G, p) \in VisProcs(M^G) \) and moreover that \( r = tempId_p^H = succ(M^G, p) \). By the specification of MutexQueue the response of a \texttt{dequeue()} operation execution by \( p \) applied to \( M^G \) is \( succ(M^G, p) \). Since \( r = succ(M^G, p) \), \( \bar{H} \in Lin(H|M) \).

To prove the theorem for \( H \) in the case under consideration, we proceed as in Case D.

**Case F:** \( H \) ends with an event on the target object \( M \) by process \( p \). The proof is analogous to the one given in Case H in the proof of Theorem 6.3 for Implementation MQFI.

**Case G:** \( H \) contains a bad MutexQueue operation. The proof is analogous to the one given in Case I in the proof of Theorem 6.3 for Implementation MQFI.

### 7.1.1 RMR Complexity

Each access procedure of Implementation MQFS incurs \( O(1) \) steps since there are no loops. In particular, the RMR complexity of each access procedure is \( O(1) \).

### 8 Conclusion

In this paper we have shown how to solve mutual exclusion for \( N \) processes using a linearizable implementation of an \( N \)-process MutexQueue object and atomic read/write registers. In doing so we have re-cast the problem of implementing and proving correct an \( O(1) \)-RMR (per-passage) queue-based mutual exclusion algorithm into the intuitively more fundamental problem of implementing the underlying queue using \( O(1) \) RMRs per operation. We have presented and proved correct two such implementations of MutexQueue, based on the mutual exclusion algorithms of T. Anderson and Craig [4, 8]. We believe that a MutexQueue implementation can also be extracted from Rhee’s algorithm [24], from the two algorithms of Lee [19], as well as from the algorithm of Mellor-Crummey and Scott [23].

It is interesting to note that the above algorithms are precisely those that achieve \( O(1) \) RMR complexity in both the CC and DSM models. Algorithms that are limited to the CC model [12, 22] tend to have a simpler structure, intuitively by taking advantage of the fact that any process can locally spin on any variable. This makes it possible for processes, in particular predecessor-successor pairs, to communicate without knowing each other’s names. In particular, in the entry protocol a process can enter the queue and signal its predecessor by applying a single atomic operation.

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7The MCS algorithm lacks the bounded exit property, and so the corresponding implementation of MutexQueue is not wait-free due to the presence of a busy-wait loop in the access procedure for the \texttt{dequeue()} operation. In particular, termination of \texttt{dequeue()} is only guaranteed if every execution of \texttt{enqueue()} is eventually followed by an execution of \texttt{isHead()} by the same process. This condition is certainly satisfied by Algorithm GQME from Section 5.
in contrast, MutexQueue contains distinct operations corresponding to these two tasks. Also, in the CC model a process in the exit protocol can wake up its successor without knowing the successor’s identity. Thus, queue-based local-spin algorithms specific to the CC model operate in a mode significantly different from the one captured by the MutexQueue data type.

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References


