Radially Staggered Bonding Technology

This new approach to fine-pitch integrated circuit bonding entails a new configuration of bonding pads on the die, dual-loop wire bonding, and a new leadframe design that minimizes wire lengths. The approach bypasses the usual obstacles to fine-pitch bonding that arise with the conventional in-line approach, thus providing appreciable die size and cost reductions with a minimal assembly cost penalty.

by Rajendra D. Pendse, Rita N. Horner, and Fan Kee Loh

Advances in silicon density have made it possible to reduce the core sizes of integrated circuit (IC) devices. However, concomitant reduction of I/O pad pitch (the pitch is typically defined as the repeat distance between adjacent I/O pads) has been hard to achieve because of packaging limitations. As a result, IC designs that are I/O intensive (so-called pad-limited designs) tend to have a die size that is significantly greater than the core size, leading to poor utilization of the silicon area. Appreciable savings in the form of greater numbers of die per wafer can be realized merely by reducing the I/O pad pitch and consequently the die size.

From the packaging standpoint, the reduction of I/O pad pitch requires improvements in the technologies used to physically interconnect the I/O pads to the package. While advanced packaging techniques do exist that permit such interconnection, such as flip chip and tape automated bonding (TAB), such techniques significantly increase the cost and complexity of the package. Wire bonding is by far the most prevalent interconnection technique in the mainstream industry-standard packages that are used for housing a large majority of ASIC and other IC devices. Quite understandably, therefore, there has been a considerable push to extend wire bonding technology to finer pitches. Some success in wire bonding pitch reduction has been achieved by the use of the so-called double-tiered package structure. However, once again, this approach increases cost and therefore is unsuitable for mainstream plastic packages that are based on leadframes with a single tier of bonding fingers.

Three broad factors are considered to be obstacles for the reduction of wire bonding pitch. First, the capillary, or the tool that carries the wire, physically occupies the space between adjacent wires, and therefore interferes with the previously bonded wire if the bond pad pitch approaches the capillary wall diameter (Fig. 1). There are physical limits to how much the
capillary wall thickness can be reduced without risking frequent breakage during production runs, and this in turn places a limit on the pad pitch. Secondly, reduction of pitch requires a proportionate reduction in the size of the bond pads and higher bond placement accuracy for the wire bonding machine. This factor leads to significant loss in yield and reliability at finer pitches as a result of bonds that are not completely contained within the bond pad, often referred to as off-pad bonds. Third is the phenomenon of wire sweep in plastic packages. Plastic packages are typically fabricated by a process known as transfer molding. During the transfer molding process, liquid resin flowing into the mold cavities at elevated temperature (usually around 180°C) causes the bonding wires to be “swept” in the direction of resin flow (Fig. 2). This phenomenon causes adjacent wires to encroach upon each other or even touch, causing electrical shorts. When the pitch is reduced, two things happen: first, since the die gets smaller, wires become proportionately longer, and second, the wire spacing is reduced. Both of these factors accentuate wire sweep, often making the part unfeasible to manufacture.

![Image](image.png)

Fig. 2. X-ray micrograph of a molded package showing wire sweep. The curvature in the wire trajectories is induced by resin flow during soldering.

In this paper, we present a new approach to reducing the effective wire bonding pitch that systematically surmounts the obstacles described above. We also present extensive assembly results on a test chip in a 208-pin PQFP package demonstrating the viability of this approach.

**Concept of Radial Staggering**

Staggering of bonding pads is a simple way to mitigate the problems of capillary interference and off-pad bond placement. A staggered configuration consists of a set of offset bond pads arranged in two rows as opposed to one row (Fig. 3). Staggering increases the direct distance between any two adjacent bond pads, allowing more room for the capillary to land without impinging on previously made bonds. It also allows the size of the bond pads to be significantly greater than the corresponding size for an inline configuration of the same effective pitch.

A configuration known as orthogonal staggering (Fig. 3b) has been previously employed in conjunction with more sophisticated double-tiered package structures. However, as depicted in Fig. 4, orthogonal staggering does not work with leadframe packages because of the geometric effect of fanout, which leads to severe wire encroachment, or even overlapping, in the corner regions. Fanout is a consequence of the fact that the pitch of bond pads on the die is typically much finer than the pitch of bond fingers on the leadframe.

Radial staggering is a geometric variation of orthogonal staggering in which overlapping of wire trajectories does not occur despite a fanout pattern of wire trajectories characteristic of leadframe packages. This is illustrated in Fig. 3c and in Fig 5. As seen in Fig. 5, adjacent wire trajectories can be placed evenly by virtue of the radial staggering arrangement on the die. In the wire bonding sequence, the outer row of pads is bonded first, followed by the inner row of pads, to prevent any interference of the capillary with the loop portion of the wire trajectory.

**Layout Method and Algorithms**

A radially staggered bond pad pattern can be designed systematically using either a graphical method or closed-form mathematical expressions incorporated in the layout code. Typically, the layout is done for one eighth of the die, then mirrored about the y-axis to get the layout for one fourth of the die, followed by successive rotations of 90, 180, and 270 degrees about the center. The resulting pad arrangement is uniform and symmetric and can be used as a universal arrangement for standard pin counts. More customized arrangements are possible and can be readily developed based on the concepts illustrated here.
**Fig. 3.** Illustration of the concept of staggering. (a) Conventional inline bond pads. (b) Orthogonally staggered bond pads. (c) Radially staggered bond pads.

**Fig. 4.** Illustration of wire encroachment when orthogonally staggered pads are used with leadframe packages.

**Fig. 5.** Radially staggered bond pad configuration for one quarter of a die.

**Graphical Method.** The graphical method is illustrated in Fig. 6. The bond pads are first arranged at the desired effective pitch in a single row; this will be referred to as the initial inline arrangement. The effective pitch is usually selected so as to cause the pad ring to “hug” the IC core; see equation 8 below.

Next, a line running parallel to the die edge and representing the second row of bonds is constructed. Then, every other pad is shifted along a radial line emanating from a convergence point until it reaches the point of intersection of the radial line with the line representing the second row of bond pads.

The convergence point can in principle be chosen to be anywhere along the y-axis. In practice, the choice of the convergence point is governed by the resulting angle of approach of the bonding wire trajectory to the bonding finger and is a function of the leadframe design (see below).

As the convergence point is moved farther down the negative y-axis, the bond pad pattern approaches the orthogonally staggered configuration. In fact, the orthogonally staggered arrangement is a special case of radial staggering with the convergence point at negative infinity along the y-axis.
The value of the offset distance between the two rows of pads is a trade-off between the need to mitigate capillary interference and the need to minimize the consumption of silicon real estate. The offset should be minimized to save silicon real estate while maintaining sufficient clearance for the capillary. Typical values for the parameters described above will be presented later in this paper.

**Analytical Method.** An alternative to the graphical method for bond pad layout is to place the pads directly at Cartesian coordinate locations calculated mathematically using the convergence point as the origin. The expressions for such placement for one eighth of the die are given below (see Fig. 6). The analysis is divisible into two categories: the first category is for odd values of $N/4$ and the second is for even values of $N/4$, where $N$ is the total pad count for the chip.

For odd values of $N/4$:
\[ x(n) = (n-1)p \]  
\[ y(n) = D \]  
for odd values of $n = 1, 3, \ldots, (N/4 - 1)/2$, and
\[ x(n) = (n-1)(D/d - 1)p \]  
\[ y(n) = D - d \]  
for even values of $n = 2, 4, \ldots, (N/4 + 1)/2$.

For even values of $N/4$:
\[ x(n) = c/2 + (n-1)p \]  
\[ y(n) = D \]  
for odd values of $n = 1, 3, \ldots, N/8$ or $(N/8 - 1)$, and
\[ x(n) = [c/2 + (n-1)p](D/d - 1) \]  
\[ y(n) = D - d \]  
for even values of $n = 2, 4, \ldots, N/8$ or $(N/8 - 1)$.

In the above equations, $n$ is the bond pad number (starting from the center and increasing towards the corner), $p$ is the effective staggered pitch (repeat distance of the outer row of bond pads), $d$ is the offset distance between the rows of pads, $D$ is defined by $D = d + H + (N/4 + 3)p/2$, where $H$ represents the pad height (to be described later), and $c$ is the spacing between the two center pads on two sides of the y-axis (the value of $c$ is chosen to be equal to the minimum inline pitch capability of the technology).

Once again, as described above for the graphical method, the layout for the entire die is obtained from the the layout for one eighth of the die by a combination of mirroring and rotation about the y-axis and the origin, respectively.

**More General Layout Schemes**

The layout methodology described above consists of two steps: placement of pads in an initial inline arrangement followed by radial shifting of every other pad towards the convergence point. The initial inline arrangement was taken to be at a uniform effective pitch, $p$. This need not be the case in general.

It is evident from Fig. 5 that with a uniform initial inline arrangement, the spacing between adjacent wires progressively decreases towards the corner. This geometric effect is particularly detrimental because wire sweep is typically most...
pronounced in the corners. This occurs because in typical transfer molds, the resin flow direction is parallel to the diagonal of the chip and is therefore perpendicular to the corner wires.

An appealing choice of the initial inline arrangement would be one in which the pads are placed at a progressively increasing spacing, in a manner that would offset the progressively decreasing wire-to-wire spacing in moving from the center to the corner pads. Such a design would appreciably reduce wire sweep. A geometric progression algorithm has been developed for the initial inline arrangement. The code for layout of progressive pads is complex because closed-form mathematical expressions are not available. This is covered in detail elsewhere.²

**Angle of Approach**

We now briefly examine the criteria for the selection of the convergence point alluded to above. Fig. 7 depicts wire trajectories for two distinct bond pad layouts representing two extreme choices of convergence point. In both cases, the design of the leadframe is held constant. In Fig. 7a, the convergence point is selected to be at the geometric center of the die and in Fig. 7b, it is selected to be a large distance away from the geometric center of the die along the negative y-axis. The angle between the wire trajectory and the bonding finger is defined as the angle of approach.

![Fig. 7. Effects on angle of approach of two different bond pad layouts corresponding to two distinct choices of convergence point. The angle of approach is the angle between the wire trajectory and the bonding finger. (a) Convergence point at the geometric center of the die. (b) Convergence point far from the geometric center along the negative y-axis.](image)

A large value of the angle of approach is likely to induce electrical shorts between a bonding wire and an adjacent bonding finger, leading to lower assembly yields. It is therefore customary to specify a maximum allowable value for the angle of approach. HP's manufacturing specification requires that the angle of approach always be lower than 10 degrees. The approach angles are unacceptably high for at least one wire in Fig. 7b, but are well within the specification in Fig. 7a.

In the more general case, the approach angles are also a function of the leadframe design. As an example, in Fig. 8, a leadframe design is shown that is different from the one shown in Fig. 7, but the choice of convergence point for Figs. 8a and 8b is identical to that in Figs. 7a and 7b, respectively, that is, the convergence point is at the center of the die for Fig. 8a and at a large distance along the negative y-axis for Fig. 8b. However, in contrast to the case shown in Fig. 7, for the case in Fig. 8 the approach angles are significantly lower for the choice of convergence point at a large distance along the negative y-axis than for the choice of convergence point at the center of the die. This is a consequence of the difference in the leadframe design between Figs. 7 and 8, and underscores the role of leadframe design in conjunction with the bond pad layout on the die in determining the approach angle in the general case.

![Fig. 8. The same die pad layouts as in Fig. 7 but with a different leadframe design.](image)

The designs of typical leadframes used in real plastic packages are very close to the case depicted in Fig. 5, and therefore, low angles of approach are achievable by using the center of the die as the convergence point. This choice was made for the design of a test chip as discussed later.
As a side note, it should be stated that in certain instances, the design of bonding fingers and the corresponding choice of a convergence point for the radial staggering of bond pads on the die can be modified or customized to minimize wire length, and thus wire inductance, when electrical performance is critical. Such custom designs prove valuable in the case of high-performance packages such as ball-grid arrays (BGAs).

It can be shown that the theoretical minimum wire length with a zero angle of approach can be achieved by selecting the convergence point at a location along the y-axis that causes the subtended angle for the corner pad to be the inverse cosine of the ratio of the effective bond pad pitch on the die to the effective bond finger pitch on the package. The theoretical analysis of the general case has been performed, but is beyond the scope of this paper. The author has developed an iterative custom layout algorithm for the coupled layout of radially staggered bond pads on the die and bond fingers on the package that minimizes wire lengths for BGA packages, which typically provide fine-pitch bond finger capability and require high electrical performance.

Implications for Pad Circuitry Layout
The radially staggered bond pad configuration has one important consequence with regard to the layout of I/O pad circuitry, a point that is not initially obvious. The bond pad is typically an integral part of a unit structure known variously as the pad cell, the pad buffer, or the I/O pad. We will refer to it as the pad cell. As illustrated schematically in Fig. 9, the pad cell consists of the I/O circuitry (such as pad drivers), the bond pad, and the ESD protection circuitry. In the conventional inline bond pad design, the pad cell is called from a library and placed automatically along the die perimeter at a repeat distance equal to the bond pad pitch. For an orthogonally staggered design, this procedure is minimally modified to include an x or y offset for every other pad cell, the value of the offset being equal to the spacing between the two rows of bond pads of the staggered configuration. However, if the bond pads have to be in a radially staggered configuration, each bond pad will not line up with the remaining portion of its associated pad cell (Fig. 10). This means that the conventional pad cell placement methodology has to be modified. It also means that an additional routing trace has to be added to connect the bond pad with its associated pad cell. These features are the subject of Article 7.

Limitations
One limitation of the radially staggered design is that two rows of bond pads are required. The second row of pads uses up space and accrues a penalty in silicon area utilization. It is clear that in designs that are marginally pad-limited, a staggered design may not result in a net reduction of die size. In the following analysis, the important case of a marginally pad-limited design is quantified, and a conditional expression is derived that can be used to determine whether a die size reduction can be achieved by resorting to the radially staggered layout.

Fig. 11 is a schematic illustration of a pad-limited IC design. In this figure, the region defined as white space is unused silicon area resulting from the fact that the inner perimeter of the I/O pad ring falls outside the outer boundary of the core. This condition occurs because the repeat distance for the pad cells (i.e., the pad pitch) is not small enough to pull in the I/O pad ring so that it hugs the core. It can be shown that the size of the white space is independent of the pad height and is expressible as:

\[ 2W = P_1 \left( \frac{N}{4} \right) - C \]  

(5)
Fig. 10. Illustration of bond pad shift caused by staggering. As a result of radial staggering, the bond pads do not line up with the associated I/O pad cells.

Fig. 11. The presence of white space identifies a pad-limited IC design.

where \( W \) is the size of the white space, \( P_i \) is the lowest qualified pitch (repeat distance of pads) for inline bonding, \( N \) is the pin count, and \( C \) is the size of the core.

A pad-limited design is defined as a design that has a non-negative white space, that is, \( W > 0 \), or, using equation 5,

\[ P_i(N/4) > C. \tag{6} \]

While the effective repeat distance can be reduced using the radially staggered layout, additional space is required to accommodate the second row of pads, as well as to accommodate a possible increase in pad height necessitated by the narrowing of the pad cell. This additional space is equal to the sum of the row-to-row spacing, \( d \), and the increase in pad height, \( \Delta H \), and can be pictured as a broadening of the pad ring. The size of the white space should be greater than the...
broadening of the pad ring or the inner perimeter of the broadened pad ring will interfere with the core. This condition can be expressed as follows:

$$2d + 2\Delta H > P_e(N/4) - C.$$  \hspace{1cm} (7)

If equation 7 holds for a given IC design, the design is deemed marginally pad-limited and a radially staggered arrangement will not result in a die size reduction. However, if equation 7 does not hold, then the radially staggered layout will reduce the die size and the layout methodology described above can be used to perform the layout. In performing the radially staggered layout, the effective pitch for the initial inline arrangement should be selected so that the pad ring hugs the core. This condition can be derived from equation 6 by replacing the inequality with an equality:

$$P_{\text{effective}} = C(4/N).$$  \hspace{1cm} (8)

If the design is severely pad-limited, the value of effective pitch calculated from equation 8 may turn out to be smaller than the smallest effective pitch supported even by the radially staggered bonding capability. In this case, the smallest supported pitch should be used as the effective pitch.

A further point should be made regarding the implications of the radially staggered design for higher pin counts. In general, the relative value of the penalty in silicon area associated with the second row of pads is diminished at higher pin counts because of the increase in the nominal value of the die size. This pin count effect is contained in the parameter N in equations 6, 7, and 8. On the other hand, the relative area penalty is much greater at lower pin counts. This effect is fortuitous, since an increasing number of ASIC designs in the pin count range well above 208 are pad-limited. The higher-pin-count designs have a significantly higher average selling price and thus provide the greatest potential for cost reduction. Such designs are currently packaged in expensive double-tiered ceramic packages. In addition to the cost reduction resulting from the reduced die size, radial staggering technology provides the interesting additional potential for reducing the cost of the package itself by making it possible to design the ICs into cheaper packages based on a single layer of dense routing as opposed to multitiered structures. This can be achieved by the iterative coupled design procedure alluded to briefly in the foregoing section.\(^2\)

**Reduction of Wire Sweep**

While radial staggering helps reduce the effective I/O pad pitch and therefore the die size, the length of wires increases proportionately, thus accentuating the wire sweep phenomenon. Table I illustrates typical wire lengths that result from reduction of die pad pitch. As a reference point, today's state of the art for transfer molding technology permits wires no longer than 4.5 mm (0.177 inch) to ensure 6σ manufacturing quality levels.

<table>
<thead>
<tr>
<th>Effective Die Pad Pitch (mm)</th>
<th>Longest Wire with Conventional Leadframe (mm (inch))</th>
<th>Longest Wire with New Leadframe Design (mm (inch))</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.110</td>
<td>4.3 (0.170)</td>
<td>3.8 (0.150)</td>
</tr>
<tr>
<td>0.090</td>
<td>5.1 (0.200)</td>
<td>4.4 (0.173)</td>
</tr>
<tr>
<td>0.070</td>
<td>5.5 (0.216)</td>
<td>4.9 (0.193)</td>
</tr>
<tr>
<td>0.050</td>
<td>6.0 (0.236)</td>
<td>5.5 (0.216)</td>
</tr>
</tbody>
</table>

The dual-looping scheme (Fig. 12) was developed to mitigate wire sweep. In this scheme, wire trajectories are placed in two different planes rather than in the same plane, thus creating a vertical gap in addition to the x-y separation between any two consecutive bond wires. Since wire displacements resulting from sweep typically occur within the same plane, the required displacement of a wire to cause shorting with an adjacent wire is effectively doubled compared to the case without dual looping, thereby considerably reducing the propensity for electrical shorts or leakage.

The separation distance between the two planes in Fig. 12 is nominally 0.125 mm (0.005 inch). Such a design is made possible by virtue of the loop height control features provided by state-of-the-art wire bonders. Loop heights are controllable to within ±0.025 mm (0.001 inch) of the nominal value. Typically, the loop height for the outer row of bond pads is chosen to be lower, and the outer row of pads is bonded first, followed by the inner row, to ensure that there is no interference between the capillary and the loop portion of the previously bonded wire. Since the loop heights and bonding sequence are programmable, the entire bonding operation can be performed in automatic mode without compromising the process throughput. The nominal loop heights used in this work were 0.400 mm (0.016 inch) for the inner row of pads and 0.275 mm (0.011 inch) for the outer row of pads.
New Leadframe Design

As is evident from Table I, a reduction of effective pitch to 0.090 mm would lead to a longest wire of approximately 5.1 mm (0.200 inch) if a leadframe with conventional design were used. We have developed a new leadframe design that has reduced the longest wire to 4.4 mm (0.173 inch), which was crucial in reducing wire sweep.

Conventional leadframes are designed using standard CAD tools that have built-in algorithms for bond finger layout. By studying the existing CAD tools, we learned that such tools likely employ a minimization of approach angles algorithm in conjunction with technology limit parameters (such as minimum bond finger width and space) to perform the layout of bonding fingers for the leadframe. The technology limit parameters are derived from the design rules supplied by the leadframe manufacturers. For example, typical design rules for leadframes produced by etching technology are 0.1 mm width and 0.1 mm space, and for leadframes made using stamping technology, they are 0.125 mm width and 0.125 mm space.

We observed that, from a mathematical standpoint, the minimization of wire lengths and the minimization of approach angles (in conjunction with the minimum width and space constraints) can be mutually conflicting conditions. This point is illustrated in Fig. 13. In Fig. 13a, the angles of approach have been minimized (they are zero degrees for all of the bond wires), whereas in Fig. 13b, the wire lengths have been minimized, but the approach angles are nonzero, and are as high as 30 degrees for some wires. While the design in Fig. 13b has appreciably shorter wires, it is unfeasible to manufacture because it violates the specification for the maximum angle of approach of 10 degrees.

After pursuing a theoretical analysis, we arrived at a straightforward (perhaps excruciatingly simple!) graphical method for the layout of bond fingers that would minimize the length of bond wires. The basis for this method is the theoretical condition that the bond fingers can be brought in closest to the center when the minimum widths and spaces reach the design rule limit values simultaneously at the tips of all bond fingers. It can be shown that this condition is attained by laying out the bond fingers so that they subtend equal angles with respect to a convergence point. This latter fact formed the basis for a simple graphical method for performing the bond finger layout. Based on this simple algorithm, a leadframe layout was performed for a 208-pin device and a bonding diagram was generated for a presumed die with radially staggered bond pads at 0.090-mm effective pitch (e.g., see Fig. 5). The approach angles were calculated for this case, and the maximum value was found to be seven degrees, well below the manufacturing specification of 10 degrees. More important, the longest wire could be reduced to 4.4 mm (0.173 inch) compared to approximately 5.1 mm (0.200 inch) for a conventional leadframe.

While the methodology has been illustrated for leadframes, it is more generally applicable to the design of other package substrates, notably high-performance ball-grid arrays. The technology limit design rules for these substrates are more aggressive (e.g., 0.05 mm width and 0.05 mm space), but significantly shorter wires are required to minimize parasitic inductance. In the above analysis, the minimization of wire length algorithm was used in place of the minimization of angle of approach algorithm, and the resulting angles of approach (verified afterwards) fortuitously fell within the 10-degree limit. This fortuitous condition does not always occur, especially in the regime of very short wire lengths and double-tiered package structures. Therefore, a systematic iterative procedure is required that judiciously employs both algorithms and involves a coupled design of the radially staggered layout on the die and the bond finger layout on the package.
Radially Staggered Bond Pads on a Die

Fig. 13. Role of leadframe design in angle of approach and wire length reduction. (a) The angles of approach have been minimized. (b) The wire lengths have been minimized. In both cases, the leadframe design rules (minimum width and spacing of leads) are the same.

Assembly Evaluations

The three key elements of the fine-pitch bonding solution described above are radially staggered bond pads, dual-loop bonding, and a new leadframe design. Extensive assembly and testing were performed to establish the feasibility of these elements. A 208-pin plastic package was used as the test vehicle.

A test chip with 208 pads (N = 208) and having a radially staggered pad configuration was designed and fabricated. The physical structure conformed to standard design rules for the current generation of the CMOS process at HP's Corvallis facility. The effective pitch, \( p \), was 0.0889 mm, the offset distance between the inner and outer row of pads, \( d \), was 0.140 mm, and the pad height, \( H \), was 0.660 mm. Since \( N/4 \) is even, equations 3 and 4 were applied with a value of \( c = 0.110 \) mm, based on the lowest inline pitch capability available at the time. Using the parameters above, the die size worked out to be 6.02 mm. Details of the chip layout can be found in the Article 7.

Daisy chains were incorporated in the design to check for leakage current between adjacent bond pads. This feature was motivated by the need to test the susceptibility to wire sweep, which is known to manifest itself as an electrical leakage between adjacent bond wires (the leakage at every bond wire can be monitored externally using the package pins).

In addition, a 208-pin leadframe was designed and fabricated by the etching method using the principle of minimization of wire length. The leadframe was fabricated by an external leadframe supplier using standard design rules and production methods.

Assembly and Test Results

The die was assembled in a 208-pin PQFP package at HP's production facility in Singapore. A dual-loop bonding process was developed and the dual looping was performed in automatic mode on production wire bonder. A simple electrical test program was used to perform package testing on a production tester to check for open bonds (continuity) and electrical leakage between adjacent pins. In addition, transmission X-ray analysis was done on finished packages to check for physical evidence of wire sweep. A final test yield exceeding 97% on two independent assembly lots was set as the criterion for acceptability of the technology in the manufacturing environment, based on inputs by the production group.

Results of the assembly evaluations are summarized in Table II. A micrograph of the dual-loop wire bonds taken before the molding operation is shown in Fig. 14. A typical transmission X-ray image of the finished package is presented in Fig. 15. While the results in Table II are considered to be well within the acceptable range, failure analysis was performed on the electrical failures from lot 1 to determine if the failures were in any way related to the fine-pitch bonding design. The details of the analysis are not reported here; it suffices to say that electrical failures were found to be unrelated to the fine-pitch bonding design and are presumed to be defects at the die level (these defects escaped, since no wafer-level testing was done on these lots), implying an effective 100% yield from the standpoint of fine-pitch bonding.
### Table II
**Assembly Parameters and Yields**

<table>
<thead>
<tr>
<th></th>
<th>Lot 1</th>
<th>Lot 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Units</td>
<td>297</td>
<td>185</td>
</tr>
<tr>
<td>Assembled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wire Diameter, mm (inch)</td>
<td>0.033 (0.0013)</td>
<td>0.033 (0.0013)</td>
</tr>
<tr>
<td>Maximum Wire Length, mm (inch)</td>
<td>4.5 (0.177)</td>
<td>4.5 (0.177)</td>
</tr>
<tr>
<td>Nominal Loop Height for Inner/Outer Rows, mm (inch)</td>
<td>0.406 (0.016)/0.279 (0.011)</td>
<td>0.406 (0.016)/0.279 (0.011)</td>
</tr>
<tr>
<td>Final Test Yield, %</td>
<td>99.3</td>
<td>98.4</td>
</tr>
</tbody>
</table>

**Fig. 14.** Typical dual-loop wire trajectories before molding.

**Fig. 15.** X-ray micrograph of a molded package (corner region).

It should be noted that the wire sweep pattern depicted in Fig. 15 is typical of production packages and shows no evidence of wire encroachment or overlapping. However, in view of the dual-loop structure, it could be argued that there will be no electrical leakage despite any overlapping of adjacent wires, since the wires are in fact spaced in the z direction. This raises the interesting possibility of potentially circumventing the effects of wire sweep altogether, especially when the technology has to be extended to much finer pitches. Therefore, we studied the effects of wire overlapping as seen in transmission X-ray observations on electrical leakage between the overlapping wires. Fig. 16 is an X-ray micrograph of a package in which significant wire movement has been induced, leading to overlapping of adjacent wires in the corner region. Electrical leakage measurements were made on ten sets of overlapping wires from three different packages. In all cases, no leakage was detected up to a limit of 10 megohms. It can be inferred from this preliminary evaluation that the 0.125 mm (0.005 inch) of z separation in the dual-loop design is perhaps adequate to prevent leakage in overlapped wires. A more detailed study is required to characterize this result fully.

**Extendability to Finer Pitches**

The migration of radially staggered bonding technology to finer pitches (below the nominal 0.090-mm effective pitch demonstrated in this study) is significantly easier with radially staggered bonding than with conventional inline bonding. This point is illustrated in Table III for the case of 0.070-mm effective pitch.
Fig. 16. X-ray micrograph of a molded package with deliberately induced wire movement leading to the appearance of overlapped wires when viewed from above.

Table III
Comparison of Wire Bonding Parameters for Radially Staggered and Inline Configurations for 0.070-mm Effective Pitch

<table>
<thead>
<tr>
<th></th>
<th>Inline</th>
<th>Radially Staggered</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad-to-Pad Distance, mm</td>
<td>0.070</td>
<td>0.095</td>
</tr>
<tr>
<td>Bond Pad Opening, mm</td>
<td>0.060</td>
<td>0.075</td>
</tr>
<tr>
<td>Wire Diameter, mm (inch)</td>
<td>0.025 (0.001)</td>
<td>0.033 (0.0013)</td>
</tr>
<tr>
<td>Free-Air Ball Size, mm</td>
<td>0.050</td>
<td>0.070</td>
</tr>
<tr>
<td>Capillary Wall Thickness, mm</td>
<td>0.030</td>
<td>0.045</td>
</tr>
</tbody>
</table>

It should be noted that reduction of the bond pad opening to 0.060 mm and the concomitant reduction in free-air ball size* to 0.050 mm required for the inline case translate to ball size control and bond placement accuracy levels that are beyond the capabilities of current wire bonding equipment, while the corresponding values for the radially staggered configuration are well within the range of equipment capabilities. Additionally, it can be shown using finite element modeling that the reduction of wire diameter from 0.033 mm to 0.025 mm translates to an approximately twofold increase in wire sweep. Finally, the reduction in capillary wall thickness will reduce the capillary life by approximately a factor of two. Thus it is clear that, in general, a finer effective pitch is achievable using the radially staggered configuration with considerably relaxed wire bonding design rules compared to the corresponding inline case.

Despite these points, a few important limitations come into play when finer-pitch extensions are considered, even with the radially staggered bonding configuration. First, the reduced die sizes resulting from finer effective pitches lead to proportionately longer bonding wires. This point was illustrated in Table I. As an example, the wire length of 5.5 mm (0.216 inch) resulting from a presumed 0.050-mm effective pitch design is considered unfeasible to manufacture because of wire sweep, based on current process specifications. It is possible that the dual-looping scheme may obviate this problem, but this needs to be evaluated. It is also possible to reduce the bond finger pitch of the leadframe (and thus the wire length) by using interposers,** but the cost and technical feasibility of this approach is so far unproven.

A second limitation is that the routing requirements for interconnection of the bond pads to the I/O circuitry and ESD structures are proportionately tighter at finer pitches and may impose some additional restrictions (see Article 7).

*A typical thermosonic gold wire bond consists of a ball bond at one end and a stitch bond at the other end. “Ball size” refers to the size of the ball that makes up the ball bond, after the ball is attached to the chip. “Free-air ball size” refers to the size of the ball as soon as it is formed, before it is attached to the chip.

**An interposer is a small circuit card that is placed between the die and the leadframe. It contains a pattern of traces that fan out from a fine pitch at the die end to a coarse pitch at the leadframe end.
A third limitation, as illustrated in Table III, is an overall tightening of wire bonding design rules dictated by reductions in pitch. In addition to the burden that this imposes on the capability of wire bonding and molding equipment, it also necessitates the development of new metrology tools and bond quality standards. Bond quality standards can only be set by a careful study of the impact of new wire bonding design rules on reliability. As an example, the smaller ball size, the finer wire diameter, and the presence of off-pad bonds may impact reliability. New specifications for these parameters can be set after the effect on reliability is well-understood. This significant effort has been recently undertaken by SEMATECH, a consortium of semiconductor companies.

Conclusions
A new approach to the reduction of wire bonding pitch is presented that entails the use of two rows of radially staggering bond pads on the die, as opposed to the conventional inline arrangement. We have combined the radial staggering methodology with dual-loop bonding and a new leadframe design, forming an integrated solution for reducing the effective wire bonding pitch and thus the die size of pad-limited IC devices. The approach has been qualified by extensive assembly evaluations of a test device in the production environment. The approach is considered advantageous over the conventional approach because it is implemented with significantly relaxed design rules and therefore with minimal assembly cost penalty.

Acknowledgments
The authors wish to thank Paul Van Loan, Chong Num-Kwee, Chong Chew-Wah, Steve Ratner, and Lynn Roylance for their technical inputs, support, and encouragement throughout the course of this project. We are also indebted to the technicians and operators whose diligence made this work a reality.

References