Frequency Modulation of System Clocks for EMI Reduction

This paper focuses on clock dithering as an on-chip technique for EMI reduction. It is a survey paper based on information gathered from inside and outside HP's Integrated Circuit Business Division (ICBD). It reviews the basic concept, the work that has been done at ICBD and elsewhere, ICBD customer experiences, and lessons drawn from these experiences about design, effectiveness, and customer implementation with ICBD.

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The proliferation of electronic products in the home and office is putting increasing pressure on every product to reduce its electromagnetic interference (EMI). At HP's Integrated Circuit Business Division (ICBD), several different methods have been used to help deal with EMI directly on-chip, among them frequency modulation of the system clock, also called clock dithering, and control of pad output rise and fall times over process, voltage, and temperature (PVT) variations. This latter method is also called adjustable output pad (AOP) control, and sometimes includes programmable adjustment for capacitive loading.

This paper focuses on clock dithering as an on-chip technique for EMI reduction. It reviews the basic concept, the work that has been done at several different ICBD design centers and elsewhere, ICBD customer experiences with that work, and lessons drawn from these experiences about design, effectiveness, and customer implementation with ICBD. The paper closes with a brief review of the costs and benefits of implementing dithering and a summary of what customers can expect when working with ICBD. This paper does not aim to be a comprehensive description of dithering circuitry and mathematics, but rather a more narrative description of experiences and rules of thumb. See **reference 1** for a more detailed discussion of circuit implementation.

Typical Clock Dithering Circuit

The key idea, illustrated by Fig. 1, is the control of the frequency of the voltage-controlled oscillator (VCO) of a phase-locked loop by appropriate division of the reference clock (RefClk) by the input divider (Q) and of the VCO clock (fvco) by the feedback divider (P). The dividers all consist of digital counters. The divided digital waveforms are compared by the phase-frequency detector, which puts out an up or down signal pulse depending on whether the P waveform lags or leads the Q waveform. The width of the up or down pulse is proportional to the amount of lag or lead. The up or down pulse is fed to the charge pump and low-pass filter block, which translates it to a change in the VCO control voltage (vcntl). The VCO control voltage is repeatedly adjusted by up or down pulses until the VCO frequency fvco is such that the P and Q waveforms align (i.e., the up and down pulses are of nearly zero width). At this point $RefClk/Q = fvco/P$. Since the VCO frequency is divided by the output divider D, the actual output signal $PllClk = fvco/D$. Thus, the output frequency at stable operation is dictated by the values of the Q, P, and D dividers, and by appropriate substitution can be written as $PllClk = P(RefClk)/(QD)$. Thus, for example, if $RefClk = 16$ MHz, $P = 50$, $Q = 10$, and $D = 5$, the output frequency PllClk is the same as the input frequency, 16 MHz.

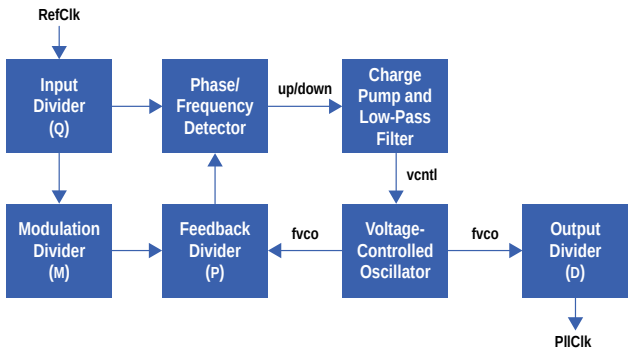

Fig. 1. *Block diagram of a typical dithering phase-locked loop.*

If the P counter endpoint is 49, the output frequency is 15.68MHz, 2% less than 16 MHz. Therefore, a simple way to achieve dithering is to change the P counter endpoint back and forth between 50 and 49 at some reasonable rate. Controlling this rate is the job of the M counter, that is, the P counter endpoint is changed each time the modulation counter (M) reaches its endpoint. A typical value for M might be 10, so that the modulation frequency is then 16 MHz/(QM) = 160 kHz. In practice, either the Q counter, the P counter, or both can be changed to achieve different target frequencies. Furthermore, by using both the rising and falling edges of the VCO clock, P can effectively have values such as 50.5 and 49.5, thus allowing a symmetric deviation of ±1% about a center value of 50.

The scheme described above can be thought of as square wave modulation because the phase-locked loop is asked to jump instantaneously from one frequency to another. Because real systems don't respond that way, and because of deliberate filtering to moderate this sudden transition, the actual frequency modulation waveform looks more like a ringing square wave. Typical simulation results for startup, lock, and modulation for this design, using the SABER analog/digital mixed-signal simulation tool, are shown in Figs. 2a and 2b. The VCO control voltage vcntl represents frequency, up and down are as described above, and p_sel is the output of the modulation divider (M). Frequency deviation of the dithered clock is typically ±1% to ±2%, and modulation frequency is typically 50 kHz to 250 kHz. Cycle-to-cycle jitter has ranged from well under 0.5% to as much as 2% for designs to date.

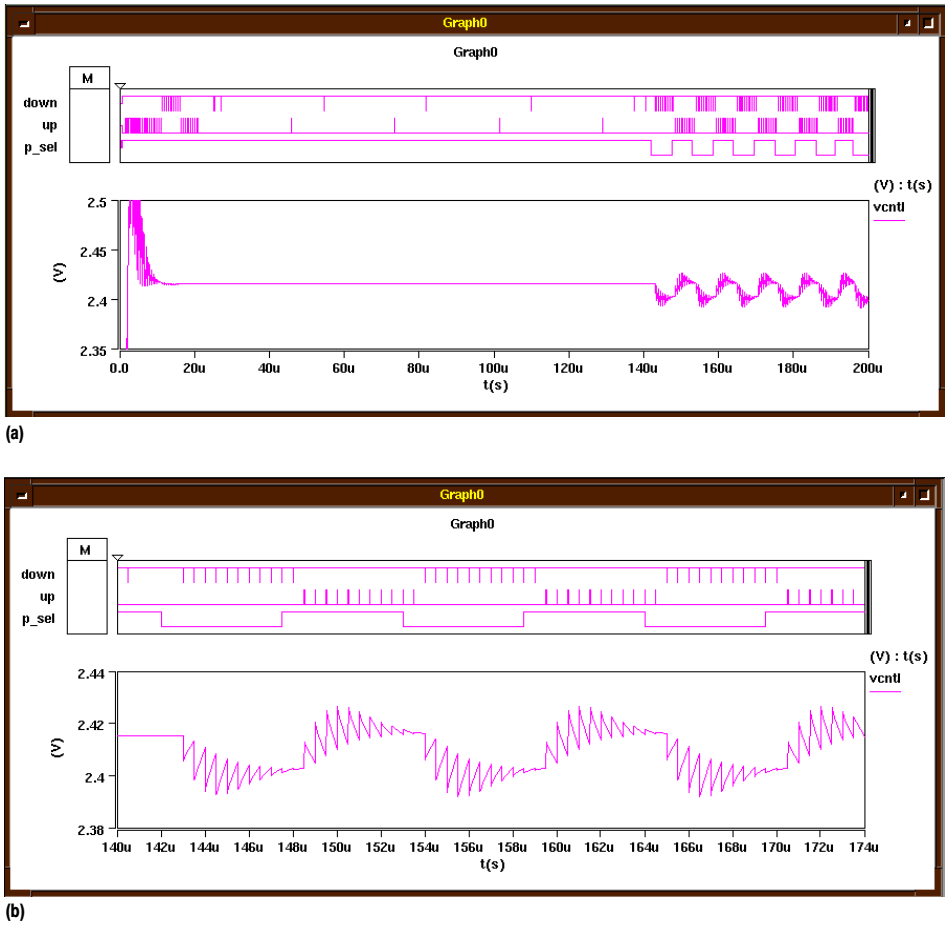

Fig. 2. *(a) SABER simulation of the startup, lock, and dithering regions of phase-locked loop operation using square wave modulation. The VCO control voltage vcntl is proportional to the output frequency. (b) Closeup of the square wave modulation waveform. Note the ringing square wave appearance.*

Square wave modulation as just described has been used successfully in a number of products to reduce EMI emission sufficiently to allow products to pass FCC testing when they otherwise could not. However, in some applications, the cycle-to-cycle jitter associated with this modulation method cannot be tolerated by the system (this is discussed further below). Over the last year this drawback has been addressed at ICBD by the development of triangle wave modulation. This method uses delta-sigma methods to step the phase-locked loop frequency more gradually from a low-frequency target to a high-frequency target and back again, resulting in what is usually called triangle wave frequency modulation. The technique greatly reduces cycle-to-cycle jitter of the phase-locked loop output clock compared to square wave frequency modulation. It also provides some improvement in EMI reduction because of flatter spectral response between the upper and lower frequency targets. This new phase-locked loop design has been successfully implemented in ICBD's CMOS14TB process on two ASICs for HP products. The new modulation method is less sensitive to process variation than previous methods, and

should therefore be easy to port to future process generations and second-source fabrication facilities. Fig. 3 shows a closeup of the triangle-wave modulation waveform of this new design (startup is similar to square wave modulation).

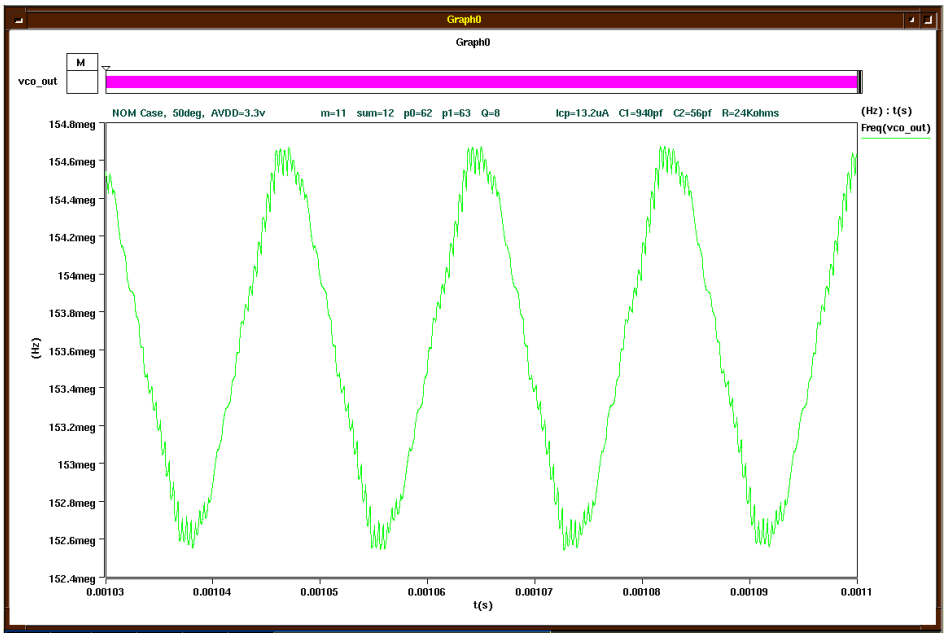

Fig. 3. *Closeup of the triangle wave modulation waveform. Startup and lock are similar to square wave startup and lock of Fig. 2a.*

HP Experiences with Dithering

ICBD Customer Divisions. A number of HP products have used clock dithering to date. For one product, two different modulation schemes were designed and manufactured by two independent organizations using different processes. For one design and process the modulation waveform looked like a ringing square wave that substantially overshot the target frequencies, while for the other design and process the modulation waveform was more triangular because of its use of a smaller-bandwidth filter. The advantage of the triangular version was that changes in period from cycle to cycle were gradual (less cycle-to-cycle period variation or jitter), and the spectrum was smoothly spread across many frequencies between the minimum and maximum. However, because the narrow-bandwidth filter loop response was so slow, for worst-case slow conditions the VCO frequency never reached its target value, limiting total frequency deviation and thus EMI reduction. In the ringing square wave version, the loop response was very fast, so that target frequencies were reached and even exceeded because of overshoot, over all process conditions. For this square wave scheme, the frequency was distributed over a wider range, although less evenly. Fig. 4 shows simulated VCO control voltage waveforms for these two different designs for qualitative comparison.

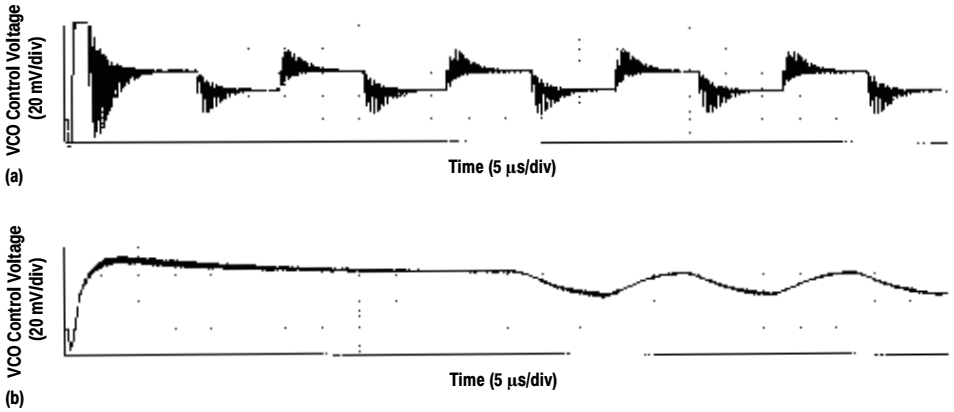

Fig. 4. *Simulated VCO control voltage plots for (a) a square wave modulation design and (b) a triangle wave modulation design. Note the longer startup and lock time for (b), reflecting its slower response.*

Conducted EMI measurements of the frequency spectrum of the system clock pin showed lower peak values for the square-wave-modulated part than for the triangular-wave-modulated part, which appeared to be a result of greater spectrum spreading because of square wave overshoot. However, radiated emissions from the boards using parts designed with triangular wave modulation exhibited less noise overall. Although the reason for this was not proved, it appeared to be the result of slower overall switching speeds of the process used to manufacture this version of the design. Nevertheless, for parts from both processes, dithering had a beneficial effect on EMI. Fig. 5 shows conducted frequency spectra for one of the harmonics of the dithered clock measured on the clock pin of each part.

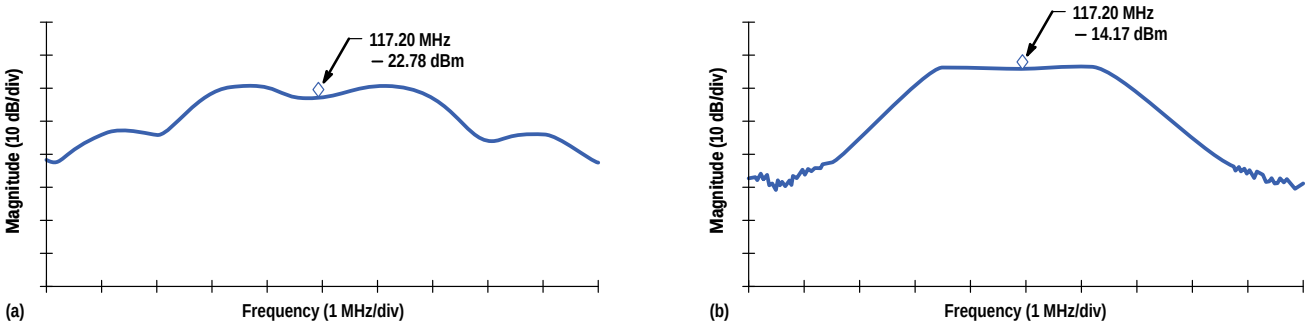

Fig. 5. *Conducted spectrum of a dithered clock harmonic for (a) a square wave modulation design and (b) a triangle wave modulation design. Spectra were filtered through a CISPR16-compliant quasipeak detector (see "**EMI Measurement Standards**" on page 6).*

For the product described above, the EMI reduction observed for square wave modulation did not seem to match the reduction predicted mathematically by standard FM theory based on the deviation and the modulation rate. Therefore, for another product, a dithering phase-locked loop using square wave modulation was made programmable to a number of different deviation and modulation values to make it possible to explore EMI reduction based on these two parameters. This gave the interesting result that EMI reduction was optimum somewhere between very slow and very fast modulation, contrary to standard FM theory. The reason for this is not really very surprising and is discussed further below (see "***Design Considerations***").

The complex relations described above between overall EMI reduction and modulation waveshape, process characteristics (e.g., intrinsic switching speeds), measurement method (e.g., conducted versus radiated spectra), and modulation rate caused substantial confusion and disagreement about which modulation method was better for EMI reduction, and was a primary stimulus for writing this paper.

Other HP Divisions. Another HP division has taken a different approach. This division developed an all-digital gate-array part that receives a 40-MHz input reference signal and outputs a clock that varies pseudorandomly near 14 MHz. This pseudo-random 14-MHz signal is then fed to an IC containing a phase-locked loop, which smooths the pseudorandom 14-MHz signal and thus effectively generates a dithered system clock. The pseudorandom 14-MHz signal is generated in a deterministic way that makes it exactly 14.31818 MHz on average, so that it can be used as a real-time clock. Modulation is synchronized to the horizontal sync signal of the video display so that no random jitter is observed in the video picture. Fig. 6 illustrates the appearance of the pseudorandom 14-MHz clock compared to the 40-MHz input clock and the ideal 14.31818-MHz clock. Two modulation cycles are shown.

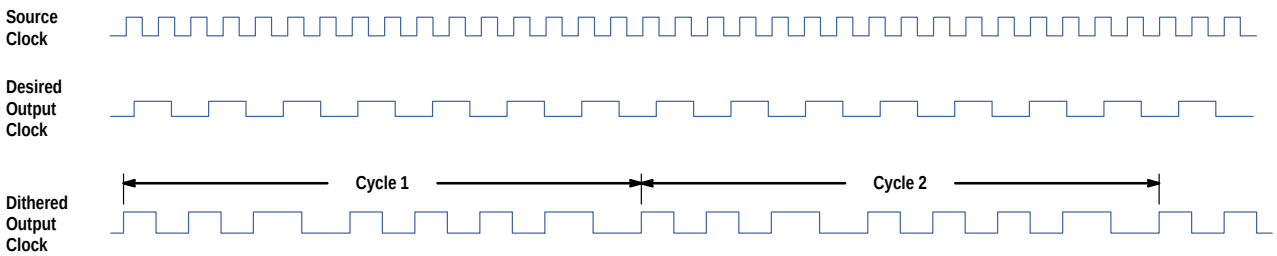

Fig. 6. *Pseudorandom clock with average frequency of 14.31818 MHz, digitally generated from 40 MHz. Two modulation cycles are shown.*

Non-HP Clock Dithering Products. A standalone product that provides a clock whose frequency varies very smoothly over various ranges of center frequency and deviation is available in the industry. However, the product is expensive, takes up board space, and requires additional surface mount parts for operation, further adding to board costs. In addition, the modulation frequency is fixed and cannot be synchronized with product operation, such as the horizontal sync signal of a

video display to prevent visual distortion due to jitter. The recently developed ICBD dithering phase-locked loops described above offer smoothly varying frequency modulation without these disadvantages, and at very low cost.

Design Considerations

EMI Reduction versus Modulation Waveform. A square wave can be described as a linear superposition of the odd harmonics of a fundamental sinusoid whose frequency is equal to the frequency of the square wave. Thus, a lot can be understood about square wave modulation of a square wave by considering square wave modulation of a sine wave. The discussion below is given with this in mind.

FM theory predicts that the power of a sine wave whose frequency is modulated by another sine wave is distributed across individual small peaks between the minimum and maximum frequency endpoints, separated by a frequency difference equal to the modulation frequency. Thus, as modulation frequency is decreased, there are more power peaks, but with lower peak values and spaced closer together. On the other hand, the spectrum of a sine wave whose frequency is modulated by a square wave contains just two peaks, regardless of how slowly the sine wave is modulated. These peaks are at the minimum and maximum frequency deviation points, and each contains half the total power of the unmodulated sine wave. This can be intuitively understood by realizing that the modulated signal spends virtually all of its time stabilized at one or the other of the two frequency endpoints.

As the modulation rate is increased, a real system designed to do square wave modulation cannot actually respond instantaneously in true square wave fashion and spends relatively more time in transition between frequencies and less time stabilized at its frequency extremes. Thus, the system starts to look more like a sinusoidally modulated system, and the two square wave power peaks tend to distribute into multiple smaller peaks. Finally, as the modulation rate is increased even further, the number of peaks will tend to decline again and their individual peak values will increase, in accordance with FM theory as discussed above.

In other words, in a real system designed to do square wave modulation there is a point of maximum EMI reduction between very fast and very slow modulation rates. The exact location of this point varies depending on phase-locked loop and product characteristics. This phenomenon was verified for the product with programmable parameters described above. For this product's particular phase-locked loop and product characteristics, measurements showed that the greatest reduction occurred at a point where the ratio of frequency deviation to modulation frequency was about 1.4.

As discussed near the beginning of this article, aside from reducing cycle-to-cycle jitter, the recent development of triangle wave modulation at ICBD also improves on the EMI reduction limitations of square wave modulation just described by more smoothly spreading spectral energy across the entire range of frequencies between the maximum and minimum endpoints at low modulation rates.

Programmability. It is valuable to provide modulation, deviation, and dithering on/off programmability in the phase-locked loop. These features should be easy to control during both phase-locked loop test mode and normal operation to allow rapid and effective evaluation of silicon and to optimize the product's EMI characteristics. This kind of characterization adds knowledge to the phase-locked loop database, and with appropriate programmability can also be used to assess product margin over a range of fixed operating frequencies.

Frequency Synthesis. Frequency synthesis is a built-in option for dithering phase-locked loops. The same basic method used to create frequencies slightly smaller or larger than the reference can be used to synthesize nearly any arbitrary frequency within phase-locked loop performance limitations. This allows the use of lower-frequency crystals (<20 MHz or so) operating in fundamental mode to generate the frequency reference. These crystals are typically less expensive, require fewer extra components, and cause fewer startup problems than higher-frequency crystals, which need to operate in overtone modes.

Spectrum Overlap. When deciding on deviation values, the designer should keep in mind the potential for spectrum overlap at higher harmonics. This can occur when the output frequency is relatively low and the frequency deviation is relatively high, and can tend to cancel out the expected EMI reduction for high-frequency components.

Mixing Dithered and Nondithered Clocks. Dithered and nondithered clock domains on the same chip usually must be treated as unrelated clock domains, and therefore should be avoided if possible. Consider the case of two clock domains, one dithered and one undithered. Given a point where the rising edges of the two clocks go up simultaneously, the edges of the dithered clock that follow will alternately lead or lag the corresponding edges of the reference clock over time. This is sometimes referred to as clock slip. Clock slip is both difficult to control accurately and difficult to measure accurately, particularly in a production environment. Designing a system with asynchronous domains is typically messy, complicated, and hard to simulate, so it should be avoided if possible. For example, in the case of video clocks, rather than have a nondithered clock to prevent visual jitter in the video, modulation can be synchronized to the horizontal sync signal. On the other hand, if separate clock domains are necessary, they can be used—they just require more careful engineering.

System Simulation. We recommend that our customers simulate a behavioral/structural Verilog model in their chip designs to catch unexpected problems. Examples of problem areas exposed when simulating with such a model are improper multiplexing and I/O control, inadequate pad drive strength for fast (system clock speed) output test signals, asynchronous interfaces, and marginal performance with respect to operating frequency.

A mixed-signal (i.e., analog and digital) simulation tool is indispensable for phase-locked loop design and simulation. The tool should have links to Verilog and C, and ideally should offer built-in FFT analysis capability, which can be useful for evaluation of the spectral characteristics of various dithering alternatives.

Multiple Phase-Locked Loops. Careful attention must be paid to systems with multiple phase-locked loops. Some major system IC components (e.g., microprocessors) contain phase-locked loops of their own, used for things such as frequency synthesis and generation of nonoverlapping clocks. These phase-locked loops must be able to track the dithering of the reference phase-locked loop's output adequately so that clock skew does not become excessive across the system. Unfortunately, assessing this phase-locked loop tracking ability in simulation can be difficult. A dithering phase-locked loop with very low cycle-to-cycle jitter (i.e., very slowly changing frequency) can help avoid the need for this simulation, and is a major reason for ICBD's development of triangular modulation.

Product Evaluation

Silicon Process Variation. Process speed can be an important factor affecting the apparent effectiveness of dithering. For current designs, process speed has a fairly strong effect on VCO gain as well as clock tree and output driver switching speed. Thus, we recommend that our customers make a point of looking at both fast and slow parts when evaluating the effectiveness of dithering.

EMI Measurement Standards. The CISPR16 EMI measurement standard is not absolute, and different measurement tools may all meet the standard yet give different results. The method by which EMI emissions are to be measured is defined by a standard called CISPR16-1.[2] This standard is intended to approximate the characteristics of typical radio-frequency receivers. For frequencies from 30 MHz to 1 GHz, power is averaged for a passband whose nominal width is 120 kHz at 6 dB. However, the standard allows passbands ranging from 100 kHz to 140 kHz at 6 dB, so results vary depending on the measurement filter chosen. Peak values that change at a rate faster than 10 to 20 kHz are ignored by using a quasipeak detector defined by the standard. The time-constant characteristics of the quasipeak detector are again given as a range of allowable values. This ambiguity in both filter and peak detector characteristics means one should be careful when comparing EMI measurements from different tests.

Conducted versus Radiated Spectra. It is important to differentiate between conducted and radiated spectra. When a probe is directly touched to the clock pin of a part, the conducted spectrum observed is a fairly direct representation of the spectral composition of the clock signal. However, when electromagnetic emissions are monitored at a distance from a finished product, the clock signal has been significantly "filtered" by the antenna characteristics of the product and the measurement environment. In other words, products act as frequency selective antennas, so conducted and radiated spectra can be and usually are quite different. This increases the desirability of phase-locked loop programmability to find optimum performance. Consequently, this also makes ease of controllability and access for measurement important.

Effectiveness as a Function of Frequency. Dithering is intrinsically more effective at higher harmonics and less effective at lower harmonics. This is simply because the absolute value of frequency deviation increases linearly with harmonic number, so that spectral energy is spread over a larger range at higher harmonics, while the width of the filter over which spectral energy is measured is fixed. Fortunately, high frequency is exactly where certain customers have their most severe problems. For example, one HP printer division tends to have many components on the printer board, and relies heavily on shielding to limit emissions. Low-frequency noise seems to be effectively contained, but high-frequency (short wavelength) noise tends to leak out through openings in the shielded box. For another HP printer division, on the other hand, low-frequency radiation turns out to be the primary noise source, at least in part because of unique resonant conditions created by printer cabling, with the result that dithering is less effective.

Dithering versus PVT/AOP. The PVT or AOP technique (defined at the beginning of this article) consists of controlling the turn-on times or the rise and fall times of IC output drivers (pads), ideally keeping these times constant over PVT variations, and sometimes adjusting for capacitive load as well. This method is also intended to keep ground bounce and signal reflections constant over PVT variations. It requires circuitry to monitor the PVT operating point of the IC (for example, by counting cycles of a free-running ring oscillator with respect to the reference clock), and then adjusting the driver or predriver current to control the drive strength or turn-on time of the driver, respectively. This technique requires considerable effort for pad design, customer simulation, and characterization of first silicon to accurately correlate the PVT reference to pad programming. With the practice of second-sourcing becoming more common, much of this work has to be repeated for each foundry. Unfortunately, EMI reduction has been negligible, at least as observed for HP DeskJet printers, a major user of this method. For these products, system clock noise has turned out to be a much greater source of EMI than pad switching noise, and system clock noise is not helped by this method. In fact, the low output resistance of typical PVT pads may encourage the transmission of system clock noise from the power net out through the output drivers and onto the product board. In summary, PVT or AOP is still believed to have potential benefit, especially for very fast-switching outputs, but is not likely to realize its potential until drive control is fairly automatic inside each pad, without requiring chip-level programming intervention.

Dithering addresses most of the limitations of PVT. The system clock tends to be the top noise source because by design everything happens at rising and falling edges of the clock. This means that clock dithering will tend to spread out all sources of noise throughout the system, since all of them are related to the clock. Thus, the advantage of dithering circuitry

is that it is essentially a single independent block that can be inserted into an IC design to help reduce EMI globally, at both chip and board levels.

Verifying Testability and Compatibility. Customers need to set aside engineering time to design their IC to make the phase-locked loop accessible for testing and to ensure that the IC will work with a dithered clock. In production testing the phase-locked loop internals are typically tested while the IC is in a special phase-locked loop test mode. During this mode certain pins of the IC are multiplexed to the phase-locked loop block's input and output ports for direct access on a production tester. Special test decks written by ICBD are then applied to the part. The customer needs to design the IC to accommodate this phase-locked loop test mode configuration. The customer also is advised to simulate the IC design at the extremes of frequency expected from the dithered clock, and to include uncertainty in the clock edge to account for cycle-to-cycle jitter. Finally, recall the earlier recommendation that if dithering is used it should be applied to the entire clock domain. If that is not possible, customer effort will be required to design asynchronous interfaces that do not rely on controlled phase relations between the dithered and nondithered clock domains.

Customer Evaluation. At this point in the evolution of clock dithering, customers should plan to spend some extra time beyond the usual EMI characterization of their product to characterize their systems with dithering. As experience is gained both by customers and ICBD, this need should decline.

Acknowledgments

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Reference

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2. *International Special Committee on Radio Interference, CISPR16-1: Specification for radio disturbance and immunity measuring apparatus and methods, Part 1*, International Electrotechnical Commission, Geneva, Switzerland. First edition 1993.

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