Timing Flexibility

Microprocessor design is a time-consuming and expensive process. Ideally, a design should scale through several fabrication process generations with low-investment algorithmic artwork shrunk to help amortize the cost of the original design.

Although it is relatively straightforward to increase the processor frequency, the frequency of interconnect to the rest of the system is more or less fixed. Typically the base processor design has the capability for a range of core-processor-frequency-to-interconnect-frequency ratios.

The PA 7300LC has three interfaces that are tolerant of increases in the processor frequency: the I/O bus interface, the main memory interface, and the second-level cache interface.

The cycle time of the general system connect (GSC) I/O bus can be configured to some multiple of the processor's cycle time. The I/O controller supports ratios from three to nine. The second-level cache controller can be configured to support a variable number of CPU cycles per second-level cache cycle. The controller supports two, three, or four CPU cycles per cache cycle. Similarly, the main memory controller can configure the setup and hold times of the DRAMs to be two, three, or four CPU cycles. Additionally, seven key DRAM timing parameters can be individually programmed.

As the processor gets faster, performance may improve but only as a sublinear function of processor frequency since memory and I/O performance remain constant. The large first-level caches on the PA 7300LC help insulate the processor from the effects of the relatively slow memory accesses, allowing the performance to scale well with increasing core processor frequency. The initial frequency target for the PA 7300LC was 132 MHz, but design ratios support core processor frequencies up to 360 MHz.

Two additional benefits are derived from the timing flexibility of the PA 7300LC. The increasing availability of higher-speed DRAMs and SRAMs makes it a simple matter to configure the timing generators to take advantage of these new components. Also, timing flexibility decouples the design effort from uncertainties that develop as RAM component vendors traverse their own development cycles.

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