Steady-state Thermal Conductivity Measurement of Dielectric Stacks for Phase-Change Memory Power Reduction

Scott W. Fong, Gary A. Gibson, Liang Chen, Aditya Sood, Mehdi Asheghi, Niru Kumari, H.-S. P. Wong

Keyword(s):

thermal conductivity; phase-change memory

Abstract:

Phase-change memory (PCM) devices require lower write power to be competitive with other memory devices. A promising method to decrease the write power required for switching is to localize heating and thus develop thermally confined devices. In this regard, it is increasingly necessary to reduce the thermal conductivity of the dielectric layer used in these device structures. In this work, we investigate the temperature-dependent thermal conductivities of alternating stacks of thin-film amorphous dielectrics, specifically SiO_2/Al_2O_3 and SiO_2/Si_3N_4. Experiments were performed using steady-state Joule-heating and electrical thermometry, while using a micro-miniature refrigerator (MMR) over a wide temperature range (100 K - 500 K). The measurements show that the amorphous thin-film stacks exhibit effective out-of-plane room temperature thermal conductivities of about 1.14 and 0.48 W / (m x K), respectively. Both of these values are lower than bulk thermal conductivities of their constituent films. Molecular Dynamics (MD) simulations show that increased scattering at the boundary between layers, and not acoustic mismatch, is the source of the increased resistance for these thin-films. Additional Finite-Element (FE) simulations show that the primary heat loss path for dash-type cells is through the dielectric and that the SiO_2/Al_2O_3 stacked dielectric films improve PCM cell heating by 42%.

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Abstract—**Phase-change memory (PCM) devices require lower write power to be competitive with other memory devices. A promising method to decrease the write power required for switching is to localize heating and thus develop thermally confined devices. In this regard, it is increasingly necessary to reduce the thermal conductivity of the dielectric layer used in these device structures. In this work, we investigate the temperature-dependent thermal conductivities of alternating stacks of thin-film amorphous dielectrics, specifically SiO_2/Al_2O_3 and SiO_2/Si_3N_4. Experiments were performed using steady-state Joule-heating and electrical thermometry, while using a micro-miniature refrigerator (MMR) over a wide temperature range (100 K – 500 K). The measurements show that the amorphous thin-film stacks exhibit effective out-of-plane room temperature thermal conductivities of about 1.14 and 0.48 W / (m × K), respectively. Both of these values are lower than bulk thermal conductivities of their constituent films. Molecular Dynamics (MD) simulations show that increased scattering at the boundary between layers, and not acoustic mismatch, is the source of the increased resistance for these thin-films. Additional Finite-Element (FE) simulations show that the primary heat loss path for dash-type cells is through the dielectric and that the SiO_2/Al_2O_3 stacked dielectric films improve PCM cell heating by 42%.**

Index Terms—**Multilayer Dielectrics, PCM, Phase-change Memory, Thermal Conductivity, Steady-state Thermometry.**

I. INTRODUCTION

UNDERSTANDING the thermal conductivity of electrically insulating materials used in nanoelectronic devices is critically important for predicting their self-heating. [Pop IEEE 2006, Cahill AIP 2014, Pedram IEEE 2006, Wong IEEE 2010] In particular, PCM requires strong thermal confinement in both the electrodes and the dielectric to retain the heat generated and thus lower the write current required [Sadeghipour itherm 2006, Russo TED2008]. Previous work has been done to reduce the heat loss through the electrodes [Wu IEDM 2011, Kim APL2008, Sood 2014]. However, the heat loss through the dielectric has often been ignored [Russo TED2008, Im IEDM2008]. Identifying and reducing the thermal conductivity of the surrounding dielectric is important for the design and simulation of PCM. [Faraclas EDL 2011, Muneer TED 2015] Additionally, the geometry or structure used has large impact on the heat generation and dissipation through the cell. [Sadeghipour Itherm 2006, Im IEDM 2008] Recent interest in dash-type or confined PCM cells has emerged because of the low power required to melt their extremely small volumes. [Im IEDM 2008, Kang IEDM 2011, Xiong Nanoletters 2013] Previous works have thoroughly studied heat generation in mushroom PCM devices, but only some analysis has been performed on dash-type cells. Additional analysis of the heat loss path for the dash-type cell is required to understand its heat retention.

In this work, the thermal conductivity of SiO_2/Al_2O_3 and SiO_2/Si_3N_4 alternating stacks of amorphous dielectrics were measured using a steady-state thermal heater and their impact in the PCM dash-type cell was simulated. The change in temperature per applied power was measured by using an electrical heater patterned onto the dielectric thin film. The measurement was performed over a wide temperature range (100 K - 500 K). From these measurements, an effective out-of-plane thermal conductivity for the different films was calculated. Additional MD simulations helped in understanding the thermal conductivity measurements. FE simulations identified the impact that the dielectric thermal conductivities have on the self-heating and primary heat loss paths of PCM dash-cells.

II. METHODS

The thermal conductivity was calculated by using steady-state electrical measurement of the changing electrical

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resistance of a Pt line cell as shown in Fig. 1. By measuring the change in electrical resistance caused by both Joule heating of the line cell and MMR stage temperature [MMR], the thermal resistance was calculated. 1-dimensional heat conduction through the Si was assumed since the line cell is long and wide (A = 100 μm × 5 μm) compared to the film thickness (L = 60 nm). Thus the effective out-of-plane thermal conductivity was calculated using the following expression:

$$R_{Thermal} = L/k_{eff}A \quad [1]$$

The effective thermal conductivity, k_{eff}, was measured for a reference film consisting of 200 nm of SiO_2, film stacks comprised of 20 alternating pairs of SiO_2 (2 nm) and Al_2O_3 (1 nm) layers, as well as 20 alternating pairs of SiO_2 (2 nm) and Si_3N_4 (2 nm) layers. Additionally, film stacks with varying thicknesses of SiO_2/Al_2O_3 bilayer pairs (with the same total stack height) were measured to examine the film thickness dependency of the thermal conductivity: 10x [4 + 2 nm], 2x [20 + 10 nm], and a 1x [40 + 20 nm] SiO_2 and Al_2O_3, respectively. The film stack depositions are explained in Section IIa. The electrical measurements are explained in Section IIb.

A. Sample Fabrication

To minimize the thermal resistance of the substrate, the samples were prepared on p-type Si wafers with low doping (R > 1 Ω-cm), owing to the higher thermal conductivity of lightly-doped Si [Asheghi JAP 2002]. The Si wafers were HF-dipped to remove their native oxide. Then, a 50 nm Al_2O_3 reference thin-film was deposited via atomic-layer deposition (ALD). The Al_2O_3 film served as an electrical isolation from the Si wafer with relatively low thermal resistance [Cahill JAP 1998]. To create the SiO_2/Al_2O_3 and SiO_2/Si_3N_4 samples, alternating layers of SiO_2 and Al_2O_3 or Si_3N_4 were deposited via ALD. Tris[dimethylamino]silane and N_2 or O_2 plasma were used for the Si_3N_4 or SiO_2 deposition, while for Al_2O_3, Trimethylaluminum and O_2 plasma were employed. After the desired thin-films were deposited, the line cells were fabricated on top by e-beam evaporating 15 nm of Pt through a shadow mask. The Pt lines served as a heater/thermometer through which electrical current was passed. Changes in electrical resistance were used to measure Joule-heating induced changes in the temperature of the Pt lines.

As an additional check on the accuracy of our thermal conductivity measurement technique, a 200 nm thick thermally grown SiO_2 on Si wafer was measured. This layer's thermal conductivity was then compared with literature values and found to match well [Cahill Rev Scit 1990]. Also, a sample with only the low doped Si and 50 nm of Al_2O_3 was created to measure the background effect of the Si wafer. As before, 15 nm Pt line cells were deposited above the films.

B. Electrical Measurements

The samples were measured in a vacuum chamber with an MMR temperature-controlled system [MMR]. The pressure during all measurements was less than $\sim 10^{-7}$ Torr. The MMR stage was cooled via Joule-Thomson expansion of 1500 psi Ar and heated via Joule-heating an embedded resistor. The MMR stage enabled temperature control of the sample between 100 K and 500K. Thermal grease (Dow Corning 340) was applied between the MMR stage and the sample to ensure low thermal contact resistance. The Pt line thermometers were calibrated by measuring their electrical resistance as a function of temperature at 15 temperatures between 100 and 500 K. For each stage temperature, the current was measured for 400 Pt line cell biases between 0 and 25 V. The current flow through the line cell and voltage were multiplied to calculate the total power. No hysteresis was observed. An example data set is shown in Fig. 2A, where the measured electrical resistance is plotted versus power. The data from voltages greater than 5 V were then used to calculate the change in electrical resistance due to applied power (slope of the electrical resistance vs. power plot) and the electrical resistance change resulting from changes in the stage's temperature at P = 0 (by linearly fitting the data). The thermal resistance as a function of line temperature could then be calculated by using the following expression:

$$R_{Thermal} = \frac{\Delta T}{\Delta P} = \frac{\Delta R}{\Delta P}\Big|_{Joule-heating} \times \frac{\Delta T}{\Delta R}\Big|_{Stage\ Heating} \quad [2]$$

Current voltage sweeps were performed on all of the samples. The measured thermal resistance for the Si + 50 nm of Al_2O_3 reference wafer is shown in Fig. 2b. To properly adjust for the series Si + Al_2O_3 film in the other samples, the thermal resistance of the reference wafer was subtracted from their data sets.

III. DISCUSSION AND SIMULATIONS

The thermal resistances were measured as described in Section IIb. Using the 1-dimensional heat conduction assumption, the effective thermal conductivity was then calculated and is shown for each of the different material stacks in Fig. 3a. Additionally, the varying layer thickness SiO_2/Al_2O_3 films and their associated thermal conductivities are shown in Fig. 3b. The temperature-dependent thermal conductivities measured are well described by T^3 polynomial fits as plotted. This is consistent with the Debye T^3 law, which shows that the thermal conductivity is dependent only on the temperature dependence of the specific heat of the phonon modes. This implies that boundary scattering is the dominant phonon scattering mechanism as it is temperature independent [Li APL 2003]. A comparison of the measured thermal conductivities at 150 K, 300 K, and 500 K is given in Table 1. The effective thermal conductivity measurements of SiO_2 match previous data from [Cahill Rev Sci 1990], showing that the technique exhibits reasonable accuracy.

As shown in Fig. 3b, a for an increased number of thinner layers (with the same total stack thickness of 60 nm) decreases thermal conductivity. The SiO_2/Al_2O_3 and SiO_2/Si_3N_4 both show a decrease in thermal conductivity compared with their respective bulk constituents. However, they do not exhibit order of magnitude decreases compared to similar metal/dielectric interfaces [Chiritescu Science 2007, Chen APL 2013]. In dielectrics such as SiO_2, Si_3N_4, and Al_2O_3, phonons are the dominant heat carriers. In order to gain some insight on the phonon coupling between SiO_2 and other

dielectrics, we perform equilibrium MD simulations, and calculate the vibrational density of states (VDOS) of amorphous SiO_2 and Al_2O_3. [Chen HTTA] We use the Tersoff potential [Tersoff PhysRevB] for SiO_2/Si_3N_4 system, and the BKS potential [Matsui 1994] for the SiO_2/Al_2O_3 system. Comparing Fig. 4a and 4b, we find the frequency spectrum of the VDOS is comparable for Al_2O_3 and SiO_2. Moreover, since the dielectrics are amorphous, the phonon modes available for heat transfer are broadened. This causes many overlapping phonon modes in which heat can travel between the two dielectrics and thus, results in minimal thermal boundary resistance. We also performed non-equilibrium MD simulations, [Chen 2014 Rsc Adv] and determine the temperature profiles across the SiO_2/Si_3N_4 and SiO_2/Al_2O_3. Fig. 4c and 4d show that there is no significant thermal boundary resistance between interfaces because of low acoustic phonon mode mismatch between these amorphous dielectrics. The decrease in conductivity of the films is thus due to a decrease in the mean free path of phonon modes because there is increased interface scattering caused by the reduced film thickness. The reduction in thermal conductivity is not caused by acoustic mismatch between the two different dielectric materials.

Dash-type phase-change memory cells [Im IEDM 2008] were simulated using 3D Finite-element simulations. The heat transfer was simulating using Fourier heat diffusion equations (eqn 3). Thermal boundary resistances were also added to the simulation and modeled using eqn 4.

$$C \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) + Q_{PCM} \quad [3]$$

$$Q'' = \frac{\Delta T}{TBR} \quad [4]$$

where C is the volumetric heat capacity, T is the temperature at each node, t is the time step, k is the thermal conductivity, Q_{PCM} is the heat generated in the PCM layer, Q'' is the heat flux between two interfaces, and ΔT is the temperature across the interface, and TBR is the thermal boundary resistance. Fig. 5 shows a breakdown of the various dimensions used as well as the boundary conditions and thermal boundary resistances used for this simulation. Table 2 shows the thermal conductivity and heat capacities used for the various materials in this simulation. The heat was modeled as a uniform heat source in the phase-change layer for 50 ns. The top and bottom surfaces (above and below the dielectric region) were held at isothermal temperatures of 300 K. Additionally, the ends of the electrode lines were treated as isothermal boundaries. The phase-transition was simulated by adding the latent heat required to change phases to the heat capacity from 890 K to 900 K (approximate melting temperature of PCM) [Liu UW 2013]. During the phase transition, the thermal conductivity values were weighted based on the fractional transformation of the phase.

With these boundary conditions, the thermal conductivity of the dielectric material was swept between 0.01 and 2 W / (m × K). The total power required (normalized to the power required for SiO_2: k = 1.4 W / (m × K)) to attain $\Delta T = 600$ K (temperature required to induce phase

transformation from crystalline to amorphous) [Liu EDL 2011] was simulated and shown in Fig. 6a. Similarly, the normalized current required is plotted in Fig. 6b.

The breakdown of the direction that the heat flows or is stored is plotted in Fig. 6c and 6d. The heat flow into the TE, BE and radially is calculated by measuring the steady-state heat flux in each of those directions. The energy stored in the PCM layer is calculated by considering the temperature change of the PCM plus the latent heat required for phase-transformation. This is calculated using:

$$Energy\ stored\ in\ PCM = V_{PCM} \cdot [C \cdot \Delta T + L_{PCM}] \quad [5]$$

where V_{pcm} is the volume, C is the heat capacity, ΔT is the average temperature change, and L_{PCM} is the latent heat of phase transition of the phase-change material. As the thermal conductivity of the dielectric decreases, the power required dramatically decreases until we reach about 0.02 W / (m × K), approximately the thermal conductivity attainable using air-gaps [Kaydoya J Chem Ref Data 1985], at which point the heat lost in the electrodes is equal to the heat loss through the dielectric

Fig. 7 shows the impact of using the multilayer SiO_2/Al_2O_3 film and the resulting temperature. When using a thermal conductivity of 0.48 W / (m × K) (SiO_2/Al_2O_3 film), a 42% improvement in heating (ΔT / Applied Power) was measured over a typical dielectric thermal conductivity of 1.4 W / (m × K) (SiO_2 film).

IV. CONCLUSION

The thermal conductivity for SiO_2/Al_2O_3 and SiO_2/Si_3N_4 alternating dielectrics was measured over a temperature range of 100 K - 500 K using a steady-state 1-D heater. The thermal conductivity of the alternating dielectrics was lower than bulk values because of increased scattering between layers. This work shows that the reduction in thermal conductivity of the insulating films by using SiO_2/Al_2O_3 oxides can result in a 42% improvement in heating efficiency. Simulations show that by further decreasing the thermal conductivity to that of an air-gap, the power required will reduce to 10 - 20% of the power required by devices with SiO_2 as the dielectric.

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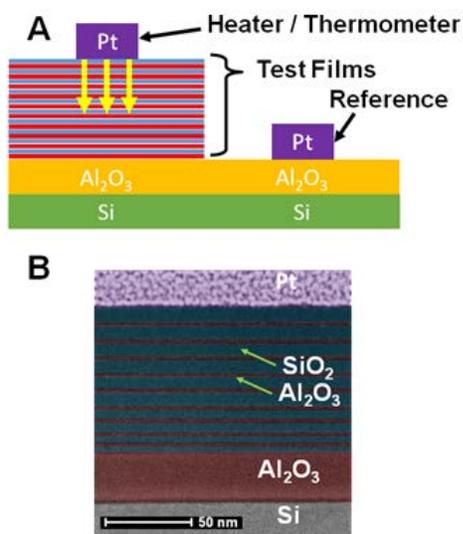
Fig. 1   A) Cross section view of the line heater/thermometer. Heat is generated in the thermometer and flows through the test film. A reference heater was also fabricated to determine the thermal resistance of the Si wafer. B). STEM image of the structure with 10x [4 nm SiO$_2$ + 2 nm Al$_2$O$_3$] Film
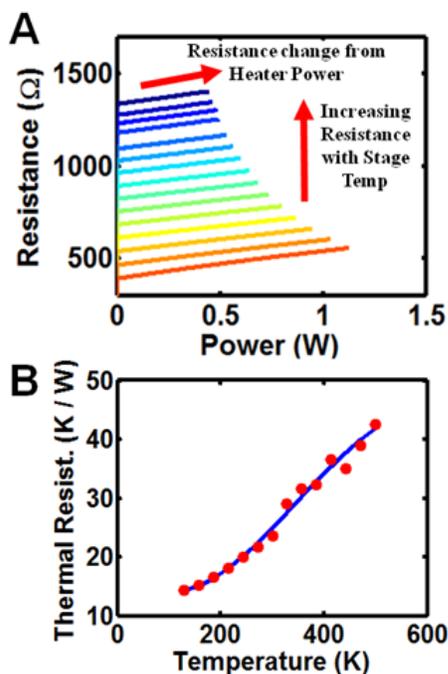

Fig. 2   A) Example plot of the measured resistance change caused by changing both heater power and stage temperature. Different colors represent stage temperatures from 100 – 500K in 15 steps. B) Measured thermal resistance of the Al$_2$O$_3$ on Si film as a function of temperature.
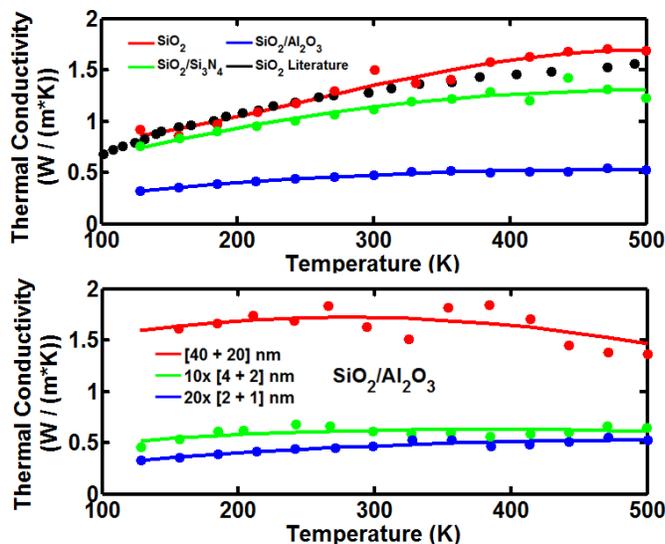

Fig. 3   A) Calculated thermal conductivities from 100K - 500K for the listed films. The films measured were 200 nm of SiO$_2$, 20 × [2 nm SiO$_2$ + 1 nm Al$_2$O$_3$] alternating layers, and 20 × [2 nm SiO$_2$ + 2 nm Si$_3$N$_4$]. B) Calculated thermal conductivities for different number of SiO$_2$/Al$_2$O$_3$ bilayers (same total thickness of 60 nm) as labeled. SiO$_2$/Al$_2$O$_3$ stacks with the thinnest film thicknesses show the lowest thermal conductivity. All measured data fit a ~T^3 polynomial curve.

TABLE I
THERMAL CONDUCTIVITY MEASUREMENTS

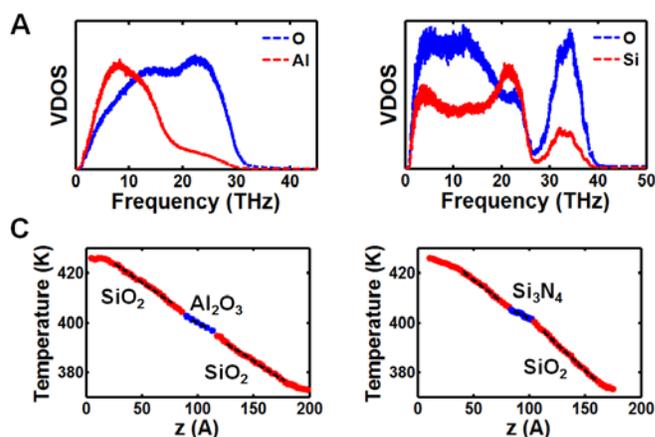| Materials	Thermal Conductivity [W/(m×K)] at Temp:		
	150 K	300 K	500 K
SiO$_2$, from [Cahill 1990]	0.9	1.3	1.6
SiO$_2$	0.9	1.35	1.69
SiO$_2$/Al$_2$O$_3$	0.35	0.48	0.53
SiO$_2$/Si$_3$N$_4$	0.80	1.14	1.23

Fig. 4   A, B) MD simulations of the phonon density of states in Al$_2$O$_3$ and SiO$_2$. C, D) MD simulations of the Temperature profile between Si$_3$N$_4$/SiO$_2$ and Al$_2$O$_3$/SiO$_2$ interfaces. Both show little thermal boundary resistance across each of the interfaces despite showing lower thermal conductivities than their bulk form.
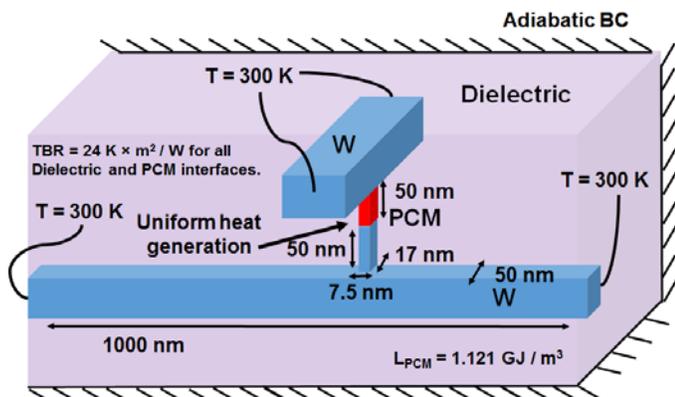
Fig. 5   Summary of the simulation boundary conditions and dimensions used to simulate the dash-type PCM cell. TBRs were included for all SiO$_2$ and PCM interfaces. [Fallica JCED 2009, Lee APL 2013] Additionally, the phase-transition was simulated using L$_{pcm}$ [Liu EDL 2011]. The parameters used for the simulation are listed in Table 2.
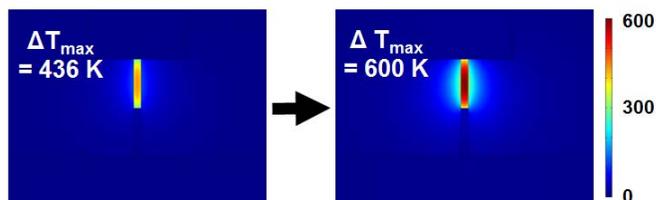

Fig. 7   Simulations of dash-type PCM cell with SiO$_2$: k = 1.4 W / (m × K) & Al$_2$O$_3$/SiO$_2$: k = 0.48 W / (m × K). Reducing the dielectric's thermal conductivity improves the heating of the phase-change layer, halving the required power to switch the device.

TABLE II
SIMULATION PARAMETERS

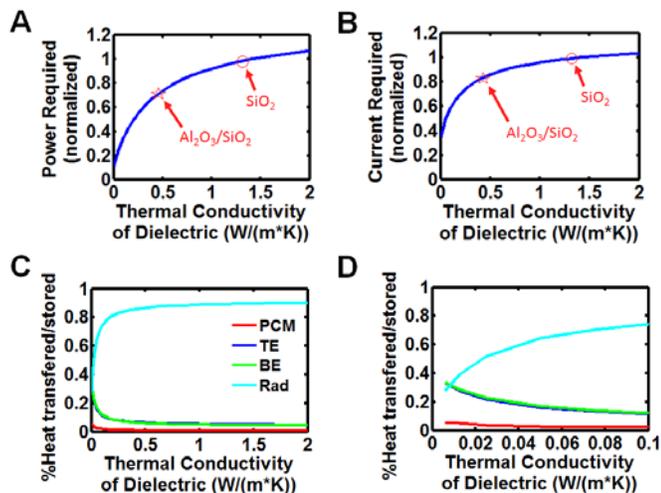| Materials	Thermal Conductivity [W / (m × K)]	Heat Capacity [J / (cm^3 × K)]
W	50 [Martan T&F 2006]	2.58 [Li TED 2012]
GST (Crystalline)	0.45 [Lee APL 2013]	1.3 [Li TED 2012]
GST (Amorphous)	0.25 [Lee APL 2013]	1.3 [Li TED 2012]
Dielectric	0.005 → 2	1.7 [Ju JAP 1999]

Fig. 6   A and B) Simulated power and current required for switching of the phase-change memory at different thermal conductivity values of the dielectric. The power is normalized to the SiO$_2$: k = 1.4 W / (m × K) case. The power required for the Al$_2$O$_3$/SiO$_2$: k = 0.48 W / (m × K) case is labeled and is 73% of the power required to switch when the dielectric is SiO$_2$. C and D) The simulated % heat lost in each direction or heat stored in the phase change layer for thermal conductivities from 0.05 → 2 and 0.05 → 0.1 W / (m × K). The energy lost radially dominates until k < 0.02 W / (m × K). This shows that continued reduction of the dielectric's thermal conductivity is necessary to improve heating of this device.