A PRECISION VERTICAL INTERCONNECT TECHNOLOGY

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Abstract
An interconnection technology is described that utilizes excimer laser drilled vias and computer controlled plating to provide vertical (Z-axis) electrical connections in high performance flexible circuits. Specifically, solid vias and hemispherical micro-contacts are created with a \( 1 \mu m \) nearest neighbor height precision for the micro-contacts. A novel structural architecture is employed which simplifies the ground plane connections for impedance controlled flex circuits. The technology is particularly suitable in the DC to 2 GHz frequency range, where large numbers of parallel connections and or multiple make and break connections are desirable. This technology was implemented with a polyimide substrate and nickel contacts, although the technology is applicable to other substrate and contact metallurgies.
INTRODUCTION

The simplest and most common form of flexible, controlled-impedance, mass interconnect media is essentially a 3-layer structure consisting of a thin dielectric substrate and two conductive layers. One of the conductive layers is usually patterned as a multitude of traces which provide electrical connections between various points of the circuit. Appropriately, it is called the circuit side. The other conductive layer on the opposite side of the dielectric substrate is often a continuous, unpatterned (or coarsely patterned), plane, which is electrically connected to the circuit's ground potential. Hence, it is known as the ground plane. A conductor trace on the circuit side in conjunction with the ground plane and the dielectric layer between them form a microstrip transmission line, whose characteristic impedance is defined primarily by the width of the conductor, and the thickness and dielectric constant of the insulating layer.

Wherever a circuit node needs to be kept at ground potential, the two conductive layers at that point must be electrically connected. Thus, a means of joining the circuit side and the ground plane through the dielectric layer is an essential feature of controlled-impedance structures. Such an element is commonly referred to as a via. Many applications also require a separable connection between the flexible circuit and other subassemblies. One solution is to create contact bumps on the flexible circuit, then press those bumps against a matching set of contact pads on the mating surface. Both the vias and the contact bumps thus have the common attribute that they conduct between circuit layers, or, conventionally, in the vertical direction. Hence, they are referred to as vertical interconnects.

A common fabrication process for both types of vertical interconnect can be achieved if the contact bumps are positioned on the ground plane side, as shown in Fig. [Ref: fg:concept]. With such an architecture, the fabrication of the via and contact bump can be done simultaneously, and involves the same two unit processes: a) making holes through the dielectric substrate, and b) back filling the holes with conductive material. In the case of vias, the filling of the hole is stopped at the surface, while for contact bumps, the deposition process is continued beyond the surface, forming the bump.

A common fabrication process is not the only advantage obtained as a result of positioning the contact bumps on the ground-plane side. One important benefit is that a rivet-like structure is created, which is mechanically sturdy and positionally stable. Another important advantage is realized when the flexible circuit is connected with a mating assembly. Referring to Fig. [Ref: fg:scheme] a, it is clear that when the contact bumps are on the ground plane side, the ground plane-to-ground plane connection is simplified. In the alternative case shown in Fig. [Ref: fg:scheme] b, it is significantly more complicated to make the ground plane connection while preserving the required impedance control.

The present article describes a fabrication technology used to create vertical interconnects (i.e., vias and contact bumps) in controlled-impedance flexible circuits. Specifically, it deals with flexible circuits based on sheet-form polyimide substrates, laminated copper films, and nickel contact bumps and vias. The rationale for material and unit-process selection will be elaborated in later sections. The article consists of three parts: Part one describes the laser drilling of holes for the vertical interconnects; part two describes the deposition of the metal interconnects; and part three characterizes the performance of the resulting structures.

The applications at which the development effort was aimed required pattern pitches on the order of 100 μm, transmission line characteristic impedances of 50 Ohms, and the use of a 25 μm thick polyimide substrate. With a dielectric constant of 3.4, a conductor trace about 43 μm wide is needed to form a 50-Ohm microstrip transmission line. The width of the conductor may vary slightly depending on its thickness. The same requirements also defined the via and bump dimensions: the via diameter were under 30 μm, while the micro-bumps were grown from 30 μm holes to reach a final diameter of 90μm.

LASER MILLING
Introduction

The fabrication of via holes for this interconnection technology required a flexible patterning capability with a minimum turn around time. Via diameters in the range of 10 to 200 μm were desired with depths greater than 25 μm. Blind via holes were fabricated on Cu clad polyimide, with the bottom of the blind via hole the inner surface of the Cu layer. This Cu layer varied in thickness from 9 μm to 35 μm and formed the starting substrate (cathode) for the subsequent via and bump plating. The smoothness of the wall was a consideration from the perspective of high yield plating, but wall taper was not a major concern. Since the vias were blind holes, with a bottom of Cu, endpoint detection was of considerable interest.

Several approaches were investigated, including wet caustic etching, plasma etching, and laser milling. The wet caustic etch is not a high precision process for vias of aspect ratios greater than 1:1 because it is an isotropic etch with the associated undercut problems. For the geometry of interest, this undercutting is a serious limitation. The plasma or reactive ion etching processes have the ability to easily achieve the required precision, but suffer from throughput and pinhole problems when etching greater than 25 μm in depth in fully cured polyimide. Based on these properties of wet caustic etching and plasma etching, as well as an interest in a maskless, direct write approach, excimer laser milling was selected as the method of choice. The laser was configured essentially as a computer controlled milling machine. This arrangement provides a very flexible patterning system that does not require the mask and resist processing steps that both plasma and wet caustic etching have.

Excimer lasers are high powered lasers that typically emit in the UV (193 - 350 nm) range. This wavelength range results in a very shallow absorption depth of less than a micron in most polymer materials. Excimer lasers run in a pulsed mode with typical pulse durations of 20 nsec. For this shallow absorption and short pulse duration, the energy per unit volume per unit time is quite high, typically $10^{11}$ joules/cm$^3$ sec.

A key factor in excimer laser processing is the fact that for wavelengths below 308 nm, the photon energy exceeds the typical carbon-carbon bond energy of about 4 eV. The implication of this is that a single photon with energy in excess of 4 eV can, in principle, directly break a carbon bond without requiring a multi-photon (i.e., thermal) absorption process. This process is thus very efficient. The bond breaking process is referred to in the literature as photochemical ablation. There has recently been a great deal of discussion in the scientific literature regarding the detailed balance between the contributions of thermal and photochemical ablation to excimer laser milling for wavelengths above 193 nm. It is, however, generally observed that even at 308 nm the character of the via holes milled by the excimer laser is very different than the character of the via holes milled by infrared lasers such as YAG or CO$_2$.

In carbon-based materials, excimer lasers tend to photochemically machine clean via holes with minimal lateral damage as opposed to visible or IR lasers that tend to melt the substrate. This effect is observed in a range of both polymers as well as biological materials.

The photochemical ablation model has several key aspects that differentiate it from the more conventional thermal absorption process. First, the photochemical ablation process exhibits a threshold effect below which energy is absorbed as heat by the substrate. Above the threshold fluence or energy density, acoustic monitoring indicates the occurrence of an explosive process that results in the ejection of material out of the illuminated zone. Computer modelling of the ablation process also supports the notion of an explosive process. At 308 nm, and high incident energy densities (> 10 J/cm$^2$) the observed lateral damage zone increases in size, indicating the effects of thermal processes as well. It is likely that at these high energy densities, nonlinear processes come into play.

Results

When this work was started there were no commercially available excimer laser machining systems that met the requirements. It was then decided to construct a system from commercially available components. The excimer laser used for this work was a model 101 MSC manufactured by Lambda Physic. The laser produced 150 mJ pulses at a 40 Hz rep rate and a wavelength of 308 nm with XeCl gas. The shot-to-shot energy stability was approximately 15%. Although the spatial variation in the fluence across the beam was about 25 %, it was found to be adequate for the ap-
plication, and a beam homogenizer was not used. The laser was incorporated into a computer controlled milling setup which is shown schematically in Fig. [Ref: fg:layout]. A computer was used to control the laser repetition rate and total number of pulses, as well as the X,Y,Z stage. The laser light was directed by two turning mirrors and illuminated an aperture plate. The first turning mirror, with an 80% reflectivity, was used to obtain a continuous monitor of the pulse energy. The approach of using an illuminated aperture plate, which is imaged onto the work piece, yields a constant fluence as the spot size is changed. Milled hole diameters in the range of 10 to 200 μm were obtained by changing the size of the aperture plate. A 2.3 mm focal length quartz lens was used to image the aperture onto the work piece. A coaxial video camera arrangement was employed to monitor the excimer milling process in situ and to enable endpoint detection by the change in plasma luminescence as the Cu interface was reached.

All of the excimer milling work discussed here was performed on 25 μm thick polyimide film [kapton]. Fig. [Ref: fg:dps] shows the depth milled as a function of the number of shots (laser pulses) for both 3 and 9 J/cm². For these two fluence levels the milling rate is different, as indicated by the value of the slope in Fig. [Ref: fg:dps]. For a fluence level of 3 J/cm², the milling rate is 0.4 μm per shot, while at 9 J/cm² the rate increases to 0.7 μm per shot. Fig. [Ref: fg:dps] illustrates that the milling rate increases with fluence level. This observation is actually in conflict with the simple photochemical ablation model which predicts that, above the energy threshold, the material removal rate should be a constant \[\text{photochem}\].

Fig. [Ref: fg:s2clr] shows the number of shots required to clear the 25 μm of polyimide as a function of fluence level. The data points at 3 and 9 J/cm² are from Fig. [Ref: fg:dps]. Although the polyimide was removed at a faster rate at higher energy densities, it was observed that the Cu surface was also damaged at these higher fluences by the excess laser shots used to ensure complete removal of the last layers of polyimide. Since the Cu surface left at the bottom of the via hole was to be used as a plating surface, the smoothness of this surface was an important criterion. Surface roughness in the Cu was found to be replicated in the plated surface. It was determined experimentally that a fluence in the range of 2 to 5 J/cm² was an optimal compromise between rapid polyimide removal and minimum Cu surface damage. The quality of the Cu surface was judged by its ability to give a smooth electroplated contact as described below. If fluence control on a per pulse basis was implemented, the polyimide could be milled at higher rates, and the fluence level reduced as the last few layers of polyimide were cleaned out of the via hole.

An SEM photo of a typical excimer laser milled blind via hole is shown in Fig. [Ref: fg:via]. This via hole is 25 μm deep (the polyimide thickness) and 30 μm in diameter. The bottom surface is the exposed Cu metal surface showing the typical surface smoothness achieved. The smoothness of the wall is indicative of the minimal lateral damage zone created by the excimer laser milling process. After excimer milling, the via holes were typically exposed to a 4%O₂ / 96%CF₄ plasma etch process to remove any residual carbon deposits and prepare the via holes for plating.

PLATING

Introduction

To bring electrical connections from the circuit side through the intermediate dielectric to the ground plane layer a deposition process is required to fill the holes created in the polyimide film with a conductive material. Different amounts of material deposition are required for the two kinds of vertical interconnects. In the case of vias, the filling of the holes stops at the surface of the dielectric layer on the ground-plane side where it makes contact with the subsequently deposited ground plane. For the contact bumps, the deposition is continued to a prescribed height above the surface of the ground plane.

Many materials and deposition techniques could, in principle, be candidates for this application. Therefore, the appropriate selections had to be made based on carefully formulated requirements. Normally, the selections of a process and a material are so tightly coupled that they must be made simultaneously. In this case, however, the process-related factors were judged clearly dominant, so the process was identified first, and then a material was selected that
Process and Material Selection

The specific requirements for the present deposition process are given in Table I.

An appropriately designed electrodeposition process meets all these requirements. It is particularly advantageous because coupled with the masking properties of the electrically insulative and chemically inert polyimide, electrodeposition becomes a naturally selective process, producing deposits only where electrical current can flow, i.e. in the laser-drilled holes. It is also the most mature and least expensive deposition processes that can be considered for the purpose at hand.

The material chosen for vertical interconnects needs to meet the process-related, as well as electrical, mechanical, and chemical requirements listed in Table II. These requirements determine the general suitability of a material for use as a vertical interconnect. However, specific applications may impose additional criteria. In the present application, the contact bumps were additionally expected to endure about $10^6$ make/break cycles, hence wear resistance was one of the most important selection factors.

A number of materials and material combinations satisfy these requirements to various degrees. Some examples are annealed copper with gold finish, hard gold, copper/nickel/gold, copper/nickel/rhodium, copper/palladium/gold, platinum, nickel. In order to make a well-founded choice, the above requirements were weighted to their importance in the application, and a matrix was constructed which ranked the scores of different materials. Using this algorithm, the material that scores highest against the listed requirements is nickel, particularly when deposited from a nickel sulfamate electroplating bath. Most of the properties of the nickel sulfamate deposit are strong functions of process and bath condition, but typical values of the parameters of interest are given in Table III.

Electrodeposition Process Requirements

In addition to the standard criteria defining a well-behaved and properly controlled electrodeposition process, additional requirements, specific to the application at hand, must be satisfied. These requirements include cleanliness, thickness control, and microstructural uniformity. The vias and contact bumps have dimensions on the order of 25 - 75 μm. Particulate or other microcontamination within the bath or in its environment can be of similar sizes and, unless removed, may cause fatal defects. In order to make a reliable contact with the ground plane, the vias must be as flush with the substrate surface as possible. Also, the heights of the contact bumps must be carefully controlled to comply with the restrictions imposed by mechanical components of the system. Both considerations require precise thickness control of the deposit. The important mechanical properties of the deposit, such as its internal stress, are dependent on microstructure. The latter, in turn, is a function of process variables. Thus, in order to maintain a uniform microstructure, the primary deposition parameters, particularly current density, must be kept constant throughout the process.

The cleanliness requirement was satisfied by including continuous filtration in the design of the bath, and by installing the plating process (as well as the associated preparatory steps) in a class 1000 clean room. In order to meet the requirements of precision thickness control and constant current density it was found advantageous to use computer control of the plating current. When plating very small features, it is customary to control the plating current and the thickness of the deposit by coating, in parallel, a much larger dummy surface. However, such arrangements are often vulnerable to geometry factors, which means that the current density on the intended features is not the same as on the dummy surface. Therefore, it was decided to plate only the desired features and to use a computer to control the actual plating current flowing through the vias and contact bumps.

Geometrical Considerations

While filling the vias, the surface area being plated remains basically constant throughout the process. But in the case of contact bumps the plating area stays constant only until the surface of the dielectric substrate is reached, then the deposit mushrooms out due to the mostly isotropic nature of the process as shown in Figure [Ref: fg:concept]. In order
Referring to Fig. [Ref: fg:geometry], for a single bump, one can derive an expression for the instantaneous area, \(a\), as a function of the instantaneous height, \(h\):

\[
a(h) = \pi r^2 (1 + \pi (h/r) + 2 (h/r)^2),
\]

where \(r\) is the radius of the seed hole in the substrate. Therefore, the current function \(i(h)\) necessary to maintain a constant current density \(J\) is:

\[
i(h) = J \pi r^2 (1 + \pi (h/r) + 2 (h/r)^2).
\]

At a constant current density the instantaneous height \(h(t)\) is a linear function of time, \(h(t) = Kt\), where \(K\) is the growth rate. \(K\) can be expressed in terms of the current density \(J\), the bath efficiency \(E\), and the charge \(Q\) necessary to grow a deposit of unit volume (a handbook value for a given material); \(K = JE/Q\). Thus, as an explicit function of time, the current required to grow the bump at a constant current density becomes:

\[
i(t) = J \pi r^2 \left(1 + \pi (Kt/r) + 2 (Kt/r)^2\right).
\]

The current necessary to plate the "stem" portion of the bump (or a via) at the same current density \(J\) is

\[
I_0 = J \pi r^2.
\]

If the thickness of the dielectric substrate is \(D\) and the height of the bump is \(H\), then the time intervals required to fill a via and to grow a bump are, respectively:

\[
t_v = D/K = DQ/JE,
\]
\[
t_b = H/K = HQ/JE.
\]

Combining Eqs. (Ref: eq:i) and (Ref: eq:I), the current function for the complete plating process can be expressed as:

\[
i(t) = \{
\begin{align*}
I_0 & \text{ for } 0 < t \leq t_v \\
I_0 \left(1 + \pi (Kt/r) + 2 (Kt/r)^2\right) & \text{ for } t_v < t < t_b
\end{align*}
\]

When the substrate contains vias and bump seed holes of \(M\) different sizes, and the number of holes in the \(k\)th group is \(N_k\), then the required current is:

\[
l(t) = \sum_{k=1}^{M} N_k \cdot i_k(t)
\]

Fig. [Ref: fg:10] shows a plot of the plating current calculated from Eq. (Ref: eq:i). The flat zone of the curve corresponds to the via plating and the quadratically increasing portion corresponds to the plating of the bump.

**Plating Current Control**
A computer-controlled power source was designed to perform two main functions. First, to supply a plating current that varies with time according to Eq. (Ref: eq:i \_t^2), and second, to provide real-time, closed-loop, automatic control of the plating current to maintain its programmed value at any time during the process. The motivation for the computer controlled plating was primarily a concern for repeatable high yield plating of small areas. The classic approach of dummy plating does not provide the sensitivity which is obtained by controlling the required current at each step of the bump plating operation. By implementing a computer controlled plating setup the ability to repeatably plate at below 1 \( \mu A \) was achieved.

The inputs to the program are: the material being plated; from which the program determines the charge per unit volume, \( Q \); and the bath efficiency, \( E \); the current density, \( J \); the substrate thickness, \( D \); the bump height, \( H \); and the number of vias and bumps in different size categories. Based on these values the program determines the plating times \( t_v \) and \( t_p \), divides the time axis into a number of short time intervals, and determines the required current in each interval. Within the plating interval, the plating current is maintained constant by using a closed-loop automatic control arrangement. The plating current passing through a sense resistor produces a voltage drop that is measured by the computer and compared to a value calculated by the program for that specific time interval. When the difference exceeds a preset tolerance, the program commands the power supply to increase or decrease the voltage as appropriate.

The algorithm which was used for the current adjustment was a compromise between the desire for rapid convergence and the tendency toward oscillation about the desired target value of the bath current. The fractional voltage discrepancy may be defined as

\[
\Delta = \frac{V_S' - V_{SO} - V_B}{V_S'}
\]

Here \( V_{SO} \) is the present source voltage, \( V_S \) is the desired source voltage, and \( V_B \) is the voltage across the plating bath. Using the voltage divider relation,

\[
V_B = V_{SO} \cdot \frac{I_B}{R_S}
\]

where \( I_B \) is the bath current, and \( R_S \) is the the resistance of the sense resistor, an expression for the required new source voltage may be derived,

\[
V_S = V_{SO} + \frac{\Delta R_S}{1 - \Delta} I_B
\]

This last equation expresses the required source voltage in terms of the measured quantities, \( I_B, \Delta \), the known quantity \( V_{SO} \) and the constant \( R_S \). The current adjustment algorithm uses Eq. (Ref: eq:Vs) to adjust the current whenever it is outside the 1% margin around the target value. With a sense resistor of 10K \( \Omega \), and a minimum addressable voltage step of 5 mV at the power supply, this control system is capable of a minimum stable current of 0.25 \( \mu A \). With a 2W sense resistor and a 20 V maximum addressable voltage of the power supply, the maximum current is about 2 mA. With a typical micro-bump requiring 0.25 \( \mu A \) to plate the stem and about 4 \( \mu A \) to finish the head, this control system was capable of repeatedly plating from 1 to 500 contact-bumps. For higher plating currents, the wattage rating of \( R_S \) may be increased.

**CHARACTERIZATION**

The vertical interconnect process described above was used in an application which required both inter-layer vias and contact bumps. Nickel was chosen as the vertical interconnect material due, in large part, to the wear resistance requirement imposed by the need for the contact bumps to endure a multitude of make/break contact cycles.

Fig. (Ref: fg:contact) shows a SEM photo of an array of the electroplated nickel contacts. These micro-contacts are 28 \( \mu m \) in height and about 90 \( \mu m \) in diameter at the base. The center to center pitch of this array is 100
Fig. [Ref: fg:dektak], shows a typical bump profile as measured by a scanning microprofilometer. This bump was plated from a 40 \( \mu m \) diameter hole to a final height of 29 \( \mu m \). The dashed line shows the calculated profile assuming isotropic plating from Eq. ([Ref: eq:area]). The sides of the bump are larger than the calculation predicts. This suggests an enhanced plating rate in this area. Contrary to the uniform plating ideal, the top of the bump is slightly rounded. This is believed to be due to nonuniform electric field lines in the plating bath, and is actually quite useful in reducing the initial contact area of the bump.

Bump height measurements were made using two different techniques, a scanning microprofilometer and a line section microscope. The results obtained with both instruments corroborated each other fairly well. It is useful, however, to note that when using a profilometer for such measurements, special care must be taken to ensure that the scan is performed precisely along a diameter, and not a chord, of the bump's base. The results obtained indicate the nearest neighbor height uniformity within the array to be better than +/- 1 \( \mu m \).

Although electroplating is capable of producing contact bumps with very high yield, specific yield problems for the plating process were observed. These were typically traceable to impurities or chemical imbalance in the plating bath. One important yield problem is a cracked bump due to excessive internal stress. This particular defect mode is due to an imbalance in the bath chemistry. A second problem is manifested by spurious growth on top of the micro-contact due to particulates in the bath. Both of these two failure modes can be eliminated by proper control and maintenance of the plating bath.

The contact resistance between the contact bumps and a mating metal surface was characterized as a function of the number of make/break operation. Fig. [Ref: fg:resist] is a plot of the results obtained from such an experiment wherein all the contacts were made by the same Nickel bump, but on different contact points on the Aluminum mating surface. A controlled amount of "scrub" motion, of about 10 \( \mu m \), was provided with approximately 5 grams of force during every contact cycle in order to ensure the removal of oxide layers and particulate contaminants. The plot demonstrates that the contact resistance remains fairly constant for \( 1.5 \times 10^4 \) cycles, at which point the accumulated and compacted debris on the bumps becomes too difficult for the scrub action to remove without additional cleaning.

It is easy to visualize that any bending or stretching of a flexible circuit containing vertical interconnect elements will subject those elements to complex mechanical stresses that may cause their failure. Therefore, it is desirable to characterize the integrity of the vias and contact bumps under such conditions. Structures containing both kinds of vertical interconnects were stretched to a strain of 5\% while the integrity of the vias was monitored electrically. The onset of failure depended on the ground plane thickness. Circuits with ground planes thicker than 2 microns survived the test repeatedly without failure. Structures with thinner ground conductors typically failed at the junction between the via and the ground film. No failures in the bumps were observed in this evaluation.

The reliability of the vertical interconnect elements was preliminarily evaluated by subjecting a small sample of circuits containing such elements to accelerated environmental testing. The test protocol is outlined in Table IV. No failures in either the vias or the contact bumps were detected after any of the above tests. Although this does not constitute a formal reliability evaluation, it gives a fairly good indication of what may be expected from such an evaluation.

CONCLUSIONS

A vertical interconnect technology for high density, controlled impedance flex circuits has been developed. The technology allows the simultaneous fabrication of interlayer solid vias and micro contact bumps using the same laser drilling and electroplating processes. Using this approach, the ground plane interconnection scheme for removable connections is greatly simplified. Structures as small as 30 \( \mu m \) in diameter were fabricated with high yield, while the nearest neighbor height variation of these structures was controlled to less than 1 \( \mu m \). Preliminary reliability evaluations indicate that these structures are very robust. Although the results reported here deal with flexible circuits, these techniques are extensible to rigid substrates as well.
ACKNOWLEDGEMENTS

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References


[kapton] The substrate film was a Cu clad kapton film of nominal 25 μ m polyimide thickness from the Fortin Corporation.

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TABLE I
DEPOSITION PROCESS REQUIREMENTS
\begin{itemize}
\item Compatibility with small geometry and materials
\item Selectivity of the deposition process
\item Adhesion of the plating to the copper traces
\item Control of the mechanical properties
\item Control of the electrical properties
\item Process maturity and low cost
\end{itemize}

\centering

TABLE II
MATERIAL PROCESS REQUIREMENTS
\begin{itemize}
\item Sufficient plating rates and thickness
\item Low electrical resistivity contact resistance
\item Low internal stresses, high elasticity modulus
\item Sufficient corrosion and wear resistance
\end{itemize}
Availability as a plating bath at acceptable cost

TABLE III
ELECTROPLATED NICKEL PARAMETERS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>RANGE</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Resistivity</td>
<td>7 - 10</td>
<td>$\mu\Omega \cdot \text{cm}$</td>
</tr>
<tr>
<td>Knoop Hardness</td>
<td>300 - 500</td>
<td>$\text{Kg/mm}^2$</td>
</tr>
<tr>
<td>Internal Mechanical Stress</td>
<td>7 - 20</td>
<td>$\text{Kg/cm}^2$</td>
</tr>
<tr>
<td>Modulus of elasticity</td>
<td>20 - 30</td>
<td>$10^3 \text{Kg/mm}^2$</td>
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TABLE IV
RELIABILITY TEST PROTOCOL

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal aging</td>
<td>125 C</td>
<td>1000 hr</td>
</tr>
<tr>
<td>Temperature/humidity</td>
<td>85 C / 85% R.H.</td>
<td>100 hr</td>
</tr>
<tr>
<td>Thermal cycling</td>
<td>-55 C / +85 C</td>
<td>20 cycles</td>
</tr>
<tr>
<td>Mechanical vibration</td>
<td>1.5 g, 10 -2000 Hz, 3 axes</td>
<td>30 min</td>
</tr>
<tr>
<td>Mechanical shock</td>
<td>500 g, 2.5 ms, 6 axes</td>
<td>10 cycles</td>
</tr>
</tbody>
</table>

Figure 1 A schematic view of the vertical interconnect structure shown in cross section.

Figure 2 Ground plane connections: a) contact bumps on the ground plane side, b) on the circuit side.

Figure 3 A schematic layout of the excimer laser milling setup.

Figure 4 The measured depth of the laser milled via hole vs the number of shots for fluence levels of 3 and 9 J/cm².

Figure 5 The number of shots to clear the via hole as a function of the fluence level.

Figure 6 An SEM photo of a 30 $\mu\text{m}$ diameter 25 $\mu\text{m}$ deep blind via hole milled at 2 J/cm². The bottom of the via hole is Cu metal.

Figure 7 A schematic drawing of the contact bump geometry.

Figure 8 A plot of the dependence of the normalized plating current as a function of the normalized bump height. $I_0$ is the stem plating current.

Figure 9 An SEM photo of electroplated Ni contact bump.
Figure 10  A profilometer trace across the diameter of a plated contact bump.

Figure 11  The contact resistance vs number of contact cycles for Nickel bumps on an Aluminum surface.