Efficient Linear RF Power Amplification with Constant Envelope Output Stages

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There is a scarcity of RF spectrum available for wireless voice and data communications. To utilize spectrum efficiently, the transmitted information is best encoded in both the amplitude and phase of the RF carrier. Transmission of amplitude modulated carriers requires linear power amplifiers. Conventional linear power amplifiers use power inefficient class A, AB or B output stages. In battery operated mobile radios power efficiency of the transmitter is of utmost importance. More efficient power amplifiers using class C or E output stages are suitable only for amplifying constant envelope carriers because of their large envelope distortion. The report describes several new methods of generating an amplitude and phase modulated carrier from two phase modulated constant envelope carriers. The carriers are produced by efficient class C or E output stages and then combined in a power combiner. The report describes also a new inherently lossless power combiner which maintains unity input power factors at all modulation levels.
1. Introduction

Wide-spread use of mobile wireless communication requires two conditions to be met:

a) Due to the general shortage of available spectrum, the RF carrier modulation by which information is transmitted must demand the smallest possible bandwidth. This means that the transmitted information should be encoded in both the amplitude and the phase (frequency) of the carrier. In order to keep the transmitted signal within the allotted bandwidth, the modulated carrier must be transmitted with minimum distortion.

b) Because a mobile radio is powered from a battery, its power consumption is very critical. If the transmitter's output amplifier is the largest power consumer in the radio, then a high efficiency power amplifier is an important design goal.

Conventional linear power amplifiers of phase and amplitude modulated carriers have class A, AB or class B output stages, which are power inefficient. There are more efficient output stages, such as class C, or E. Their higher efficiency occurs because the amplitude of the voltage swing on the transistor collector is equal to the power supply voltage. This leaves only a small voltage across the output transistor when it carries maximum current and thus minimizes the power dissipated in the transistor. To maintain high efficiency these output stages must be driven by a fixed amplitude input signal sufficient for the full swing output voltage. An attempt to achieve an amplitude modulated output by driving these stages with an already amplitude modulated input signal leads to gross envelope distortion and loss of efficiency. Class C and E stages are therefore most suitable for amplifying constant envelope, only phase or frequency modulated carriers.

An attractive method of amplifying phase and amplitude modulated signals linearly but efficiently is to amplify a phase modulated constant envelope carrier in a high efficiency class C or E output stage and to achieve amplitude modulation in a subsequent operation.

One method to accomplish the above is called "Envelope Elimination and Restoration" [2]. Here the input signal is processed in parallel by an amplitude detector and a limiter. The envelope produced by the detector is amplified in a low frequency power amplifier and the amplifier's output is used as the power supply of a, say, class C output stage. The class C stage is driven by the limited, but still phase or frequency modulated input signal. The amplitude of the class C stages' output signal follows the envelope represented by the varying output of the low frequency amplifier. The voltage across the output transistor, when the transistor carries maximum current, remains small regardless of the amplitude modulation; power dissipation in the transistor thus remains low. The disadvantage of this method is the need for the low frequency power amplifier.

Another method of achieving linear power amplification while using class C or E output stages is known as "High Power Outphasing Modulation" [1] or "LINC - Linear Amplification with Nonlinear Components" [6]. In this method a phase and amplitude modulated carrier \( v = q(t)V_{\text{max}}\sin(\omega t + \phi(t)) \) is being produced. Here \( V_{\text{max}} \) is the carrier's...
amplitude at its envelope peak, \( q(t) \) is the fractional amplitude modulation, and \( \varphi(t) \) is the carrier's desired phase modulation. To achieve high efficiency, two constant envelope, phase modulated components \( v_1 = V \sin[\omega t + \varphi(t) + \alpha] \) and \( \sin[\omega t + \varphi(t) - \alpha] \) are supplied by two constant envelope output stages and then vectorially combined in a power combiner. The additional phase modulation \( \alpha \) of \( v_1 \) and \( v_2 \) is introduced to achieve the desired amplitude modulation \( q(t) \). [In this report the explicit sign of time dependence \( (t) \) is used to distinguish independent, externally imposed time varying values from internally generated time varying values, such as \( \alpha \).] If the power combiner generates the output signal \( v \) by vectorially adding \( v_1 \) and \( v_2 \) (see Fig. 1a), then \( V_{\text{max}} = 2V \). If the power combiner generates the output signal \( v \) by generating a vector average of \( v_1 \) and \( v_2 \) (Fig. 9), then \( V_{\text{max}} = V \). In both cases the amplitude modulation will be \( q(t) = \cos \alpha \). If \( v_1 \) and \( v_2 \) are in phase, i.e. \( \alpha = 0 \), the resulting output has its maximum amplitude \( V_{\text{max}} \). When \( v_1 \) and \( v_2 \) are in antiphase, i.e. \( \alpha = 90^\circ \), the resulting output has zero amplitude. But the power combiner could also be designed to vectorially subtract \( v_1 \) from \( v_2 \) (see Fig. 1b), in this case \( q(t) = \sin \alpha \). (Phase modulation \( \varphi(t) \) of output \( v \) is achieved by rotating both \( v_1 \) and \( v_2 \) in the same direction. This can be easily visualized by imagining the phase modulation rotating the entire reference plane.)

One subject of this report is a new method of generation of carriers \( v_1 \) and \( v_2 \). Another subject of this report is a new power combiner combining the outputs \( v_1 \) and \( v_2 \) of the two constant envelope output stages. Both subjects are protected by U.S. patents granted to HP [3],[4].

In all of the following discussion we will assume that the bandwidth of the phase modulation \( \varphi(t) \) and of the amplitude modulation \( q(t) \) is much smaller than the carrier frequency \( \omega \).

2. Generation of Carrier \( v_1 \) and Carrier \( v_2 \)

2.1 Previously Published Methods

Several methods of generating the two carriers in LINC power amplifiers have been published in the past.

In [5] the two carriers \( v_1 \) and \( v_2 \) are produced starting with a low carrier frequency \( (\omega_1 < \omega) \) and low power version of the desired phase and amplitude modulated output signal \( v \), i.e. with \( v_{\text{in}} = q(t)V_{\text{inmax}} \sin[\omega_1 t + \varphi(t)] \). This signal is digitized and digital signal processing is used to generate Cartesian components \( I_1, Q_1 \), representing \( v_1 \), and \( I_2, Q_2 \), representing \( v_2 \), both at the lower frequency \( \omega_1 \). Then, with an RF oscillator, a phase shifter and mixers the two sets of \( I \) and \( Q \) components are upconverted to frequency \( \omega \). Next the related \( I \) and \( Q \) components are combined into the constant envelope.
components $v_1$ and $v_2$. Those are then driving two highly efficient constant envelope output stages which, in turn, feed the power combiner.

In [6] the angle $\alpha = \arcsin q(t)$ is produced in the following way. Similarly to [5], the starting point is a low power version $v_{in} = q(t)V_{inmax}\sin[\omega t + \varphi(t)]$ of the desired ultimate phase and amplitude modulated signal, but in contrast to [5], at the final frequency $\omega$. This signal is processed by a limiter to generate a constant envelope, phase only modulated signal $u = U\sin[\omega t + \varphi(t)]$, and in an envelope detector to generate a baseband replica of the amplitude modulation $q(t)$. Then a feedback loop is created which includes a phase modulator feeding a phase detector. The phase modulator modulates the signal $u = U\sin[\omega t + \varphi(t)]$ from the limiter by an amplified error signal causing the phase detector output to follow $q(t)$. This implements an inverse sine function so that the signal at the input of the phase modulator, when reproduced by the constant envelope output stage, is $v_f = V\sin[\omega t + \varphi(t) + \alpha]$, where $\alpha = \arcsin q(t)$. Signal $v_2$ is derived in a similar way.

The subject of [7] is essentially the same method as described in [6], except frequency multiplication is used in order to decrease the phase modulator's operating range. The phase modulator is driven by a frequency equal to one third of the operating frequency ($\omega/3$), its output frequency is then multiplied by 3 to $\omega$ in a frequency multiplier. Because phase changes are multiplied by frequency multiplication, this operates the phase modulator over a third of the ultimate phase angle range $\alpha$ and thus improves its linearity.

In [8] the amplifier first separates the input signal $v_{in} = q(t)V_{inmax}\cos[\omega t + \varphi(t)]$ by limiting and amplitude detection into a fixed amplitude phase modulated signal $u = U\cos[\omega t + \varphi(t)]$ and a baseband envelope signal $v_b = q(t)V_{inmax}$ (similar to [6]). The envelope signal is then modified by analog signal processing which includes squaring and square rooting circuitry. The limited signal is phase shifted by $90^\circ$ to $u' = U\sin[\omega t + \varphi(t)]$ and then amplitude modulated by the modified envelope signal. The original signal $v_{in}$ and the amplitude modulated signal $u'$ and its inverse $-u'$ constitute the respective $I$ and $Q$ components of $v_1$ and $v_2$. The final step is then generating $v_1$ and $v_2$ by proper summing and subtracting their $I$ and $Q$ components.

Finally, in [9], the starting point are the baseband $I$ and $Q$ components of the desired output signal $v = q(t)V_{max}\cos[\omega t + \varphi(t)]$ and a carrier of frequency $\omega$. In this amplifier, low power versions of $v_1$ and $v_2$ are generated by two voltage controlled oscillators (VCOs) and then amplified in two constant envelope output stages. The vector-summed output signal of the two stages is then decomposed by two mixers and the carrier $\omega$ into $I$ and $Q$ baseband components. Finally these $I$ and $Q$ components are compared with the original input $I$ and $Q$ signals. Any error between them is amplified and drives the VCO frequency control inputs, forcing the error to zero.

The disadvantage of the previously published methods are that any potential phase or amplitude error in some of the processing circuits, in the constant envelope output stages and the combiner appear as distortion in the ultimate output signal (except in [9]). A further disadvantage of some above amplifiers is that they cannot simply substitute a
conventional RF power amplifier because the input is either in baseband $I,Q$ form [9] or the input frequency is lower than the output frequency to either match the limited speed of the digitizer and the digital signal processor [5] or to decrease the analog processing errors [7]. Some amplifiers require complex and error prone open loop analog signal processing such as squaring and square rooting [8]. The disadvantage of the approach in [9] is that for a continuous $>180^\circ$ range of phase modulation $\varphi(t)$ of the final output signal, the amplifier must be complemented by a switching matrix operating on the input $I$ and $Q$ components. This matrix is not described in [9].

2.2 The Proposed New Method

The new method includes the advantage of [6], i.e. the input signal is a low power version of the desired output signal, so that the method can easily substitute conventional linear power amplifiers. It also includes the advantage of [9], i.e. the constant envelope output stages and the power combiner are part of a feedback loop and their error is being attenuated by the loop gain. However, the proposed new method shares the disadvantage of [2], [6], [7], [8], in that it is suitable only for modulation schemes such as Offset-QPSK or $\pi/4$-QPSK in which the carrier amplitude never drops below a specified minimum. Below certain input level the limiter would lose its output signal and phase reference would be lost. A block diagram of the new method is shown in Fig.2. The apparent complexity of Fig.2 is misleading; many of the blocks shown can be merged into relatively simple circuits. For example, addition can be implemented by summing signal currents, inversion can be done by crossing wires in differential circuits.

The new method first separates the phase modulation and amplitude modulation of the low power input signal $v_{in} = q(t)V_{in\max}\sin(\omega t + \varphi(t))$, as in [6],[7] and [8], by Limiter 1 and Envelope Detector 1.

The output of Limiter 1, i.e. signal $u_l = U\cos(\omega t + \varphi(t))$ carries the same phase modulation as the input signal $v_{in}$ but has a constant envelope. Two-quadrant multiplier $M_2$ multiplies signal $u_l$ with single polarity baseband signal $v_y$ and feeds the product, $v_{M2}$, to the first inputs of summing circuits $S_1$ and $S_2$. Signal $u_l$ is also advanced by the $90^\circ$ phase shifter. Its output signal $u_q$ is multiplied by $M_1$ with $v_x$ and fed as $v_{M1}$ to the second input of summing circuit $S_1$. Signal $v_{M1}$ is also fed to the second input of summing circuit $S_2$ via unity gain inverting amplifier "-1". The outputs of the summing circuits drive the two constant envelope output stages OS1 and OS2 via Limiter 2 and Limiter 3 respectively. These limiters guarantee that the output stages are driven by constant amplitude signals. The constant envelope outputs $v_1$ and $v_2$ of OS1 and OS2 are combined in the Power Combiner into a single amplitude and phase modulated output signal $v$ feeding the antenna or some other load. Output signal $v$ of the Power Combiner is fed also via the Attenuator to Envelope Detector 2 which generates a baseband signal $v_{b2}$ equal to the amplitude modulation envelope of the attenuated output signal $v$. The attenuation of the Attenuator is equal to the circuit's desired overall voltage gain $G$, i.e. $G = V_{\text{max}}/V_{\text{in\max}}$. Similar to Envelope Detector 2, Envelope Detector 1 generates a baseband signal $v_{b1}$ equal to the
amplitude modulation envelope of the input signal $v_{in}$. The two baseband signals are compared in high gain differential amplifier OA1 with complementary outputs X and Y.

In case $v$ is generated as the vector sum or vector average of $v_I$ and $v_2$ (as shown in Fig.2), the voltages on outputs X and Y are described as:

$$v_y = V_o + A_I v_a \quad \text{and} \quad v_x = V_o - A_I v_a$$

(1)

In case $v$ is generated as the vector difference of $v_I$ and $v_2$, the voltages on outputs X and Y are described as:

$$v_y = V_o - A_I v_a \quad \text{and} \quad v_x = V_o + A_I v_a$$

(2)

where $A_I >> 1$ is the gain of amplifier OA1, $V_o$ a common mode voltage, and $v_a = v_{b1} - v_{b2}$, i.e. the differential input voltage of amplifier OA1.

It follows from (1) and (2) that for any $v_o$ the sum of $v_x$ and $v_y$ is $v_x + v_y = 2V_o$. Voltage $v_x$ is driving the baseband input of multiplier $M_1$, voltage $v_y$ drives the baseband input of multiplier $M_2$.

The common mode voltage $V_o$ is chosen so that even the smallest rf voltages $v_{S1}$ and $v_{S2}$ passed by summing circuits $S_1$ and $S_2$ (i.e. when $v_o = 0$ and $v_x = v_y = V_o$), are still sufficiently large to drive Limiters 2 and 3 into saturation.

We will now describe the operation of the amplifier in Fig.2 using the vector diagram shown in Fig.2a. We assume again that the input signal $v_{in}$ is only amplitude modulated, and has no phase modulation. Vector $u_I$ represents the fixed amplitude output of Limiter 1. Vector $u_q$ represents the output of the phase shifter, i.e. $u_I$ advanced by 90°. Vectors $v_{M1}$ and $-v_{M1}$ are the voltages on the first inputs of summing circuits $S_1$ and $S_2$, and vector $v_{M2}$ is the voltage on the second inputs of $S_1$ and $S_2$. With the two inputs of summing circuits $S_1$ changing with $v_x$ and $v_y$ in a quasi-complementary fashion, the end-point of vector $v_{S1}$ will move along the locus $loc_{v_{S1}}$. The same applies for summing circuit $S_2$ and locus $loc_{v_{S2}}$. However, the outputs of Limiters 2 and 3 have constant amplitude, and are amplified by the output stages OS1 and OS2 that have fixed, matched gains. The loci of the end-points of vectors $v_I$ and $v_2$  are $loc_{v_I}$ and $loc_{v_2}$.

As mentioned above, in Fig.2 output voltage $v$ results from vector addition or vector averaging of $v_I$ and $v_2$ in the Power Combiner. The amplitude modulation loop works as follows. If the envelope of the output carrier $v$ is smaller than $G$-times the envelope of the input signal $v_{in}$, baseband voltage $v_{b2}$ will be lower than $v_{b1}$. This will increase $v_y$ and decrease $v_x$ at the outputs of amplifier OA1 [see equation (1)]. As the result the magnitude of vector $v_{M2}$ in Fig.2a will increase, and the magnitude of vectors $v_{M1}$ and $-v_{M1}$ will decrease. Phase angles $\alpha$ will decrease, and the envelope of output voltage $v$ will increase until the difference between $v_{b1}$ and $v_{b2}$ is negligibly small. The opposite will happen if the envelope of output signal $v$ increases above $G$-times the envelope of input signal $v_{in}$.  

5
If the Power Combiner generates output voltage \( v \) as the difference between \( v_1 \) and \( v_2 \), the operation of amplifier OA\(_1\) follows equation (2), and a too small envelope of output signal \( v \) will cause a decrease of \( v_y \) and an increase of \( v_x \), again correcting the envelope error.

We shall now examine the open loop gain in the amplitude control loop represented by Fig.2. Again, in Fig.2 voltage \( v \) is the vector sum or the vector average of \( v_1 \) and \( v_2 \). In both cases the maximum amplitude of \( v \), i.e. for \( \alpha=0 \), is denoted as \( V_{\text{max}} \). From Fig.2a:

\[
\tan \alpha = \frac{v_{M1}}{v_{M2}}
\]  

(3)

and if multipliers \( M_1 \) and \( M_2 \) are linear, then from (1):

\[
\tan \alpha = \frac{v_x}{v_y} = \frac{(V_o-A_1 v_a)}{(V_o+A_1 v_a)}
\]  

(4)

It was stated above that for generating \( v \) by vector summing or averaging the fractional amplitude modulation is \( q(t)=\cos \alpha \).

Using the trigonometric identity \( \cos x = \sqrt{1+(\tan x)^2} \) we get for \( q(t) \):

\[
q(t) = \frac{1}{\sqrt{1+[(V_o - A_1 v_a)/(V_o + A_1 v_a)]^2}}
\]  

(5)

If we write for brevity \( p=A_1 v_a/V_o \), then:

\[
q(t) = \frac{1}{\sqrt{1+[(1-p)/(1+p)]^2}}
\]  

(6)

The dependence of \( q(t) \) on \( p \) is depicted on Graph 1.

To guarantee stability and accuracy of the amplitude modulation loop it is important to check the variation of its open loop gain \( H_a \) over the amplitude modulation range \( q(t) \). If we test the loop by cutting it at the negative input of amplifier OA\(_1\), the open loop gain is \( H_a=\frac{db_2}{dv_a} \). The signal \( v_{b2} \) at the output of Envelope Detector 2 is \( v_{b2}=q(t)V_{\text{max}}/G \), where as before, \( V_{\text{max}} \) is the output voltage \( v \) with \( \alpha=0 \) and \( G \) is the attenuation of the Attenuator. When checking only the relative variations of \( H_a \) vs. \( q(t) \), we can neglect the constants \( V_{\text{max}}, G, A_1 \) and \( V_o \) and write \( H_a=\frac{dq(t)}{dp} \).

The following table gives \( H_a \) normalized to its maximum value which occurs at \( q(t)=0.5 \).
<table>
<thead>
<tr>
<th>$q(t)$</th>
<th>$H_a$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>64%</td>
</tr>
<tr>
<td>0.2</td>
<td>83%</td>
</tr>
<tr>
<td>0.4</td>
<td>96%</td>
</tr>
<tr>
<td>0.5</td>
<td>100%</td>
</tr>
<tr>
<td>0.6</td>
<td>94%</td>
</tr>
<tr>
<td>0.8</td>
<td>74%</td>
</tr>
<tr>
<td>0.9</td>
<td>50%</td>
</tr>
<tr>
<td>0.97</td>
<td>26%</td>
</tr>
<tr>
<td>1</td>
<td>0%</td>
</tr>
</tbody>
</table>

Graph 2 depicts $H_a$ vs. $q(t)$ in more detail. The open loop gain $H_a$ remains within a comfortable 2:1 ratio for a modulation range $q(t)$ from zero to 0.9. This corresponds to a range of phase angles $\alpha$ from 90° to approx. 26°. It is desirable to extend the range of $\alpha$ to the lowest possible values to achieve the largest $V_{max}$ from a given output amplitude $V$ of the constant envelope output stages. With a lower range edge of $\alpha=26^\circ$, $V_{max}=1.8V$ and $V_{max}=0.9V$ with vector summing and averaging respectively, while the variation in modulation open loop gain $H_a$ is 2:1 worst case. The modulation range of $\alpha$ is limited at the high end [i.e. at low $q(t)$] by Limiter 1 which does not tolerate an input envelope level below a certain minimum.

2.2.0 Phase Correction

When describing the amplifier operation in 2.2.1, we assumed that input voltage $v_{in}$ is only amplitude modulated, i.e. that it has zero phase modulation. If we now allow that $v_{in}$ is also phase modulated, i.e. $v_{in}=q(t)V_{inmax}\sin(\alpha t+\phi(t))$, then the whole vector diagram in Fig.2a rotates with $\phi(t)$ and nothing in Fig.2a needs to be changed. A phase difference between input voltage $v_{in}$ and output voltage $v$, caused for example by a fixed or slowly varying delay in all circuits between Limiter 1 and the output of the combiner, is also of no concern. However, any modulation dependent dynamic parasitic phase shift in the circuit elements of Fig.2 would distort the power amplifier's output spectrum.

2.2.1 Phase Correction Version 1

Amplifier performance can be improved by adding to amplifier shown in Fig.2 a phase correction loop, see Fig.3. This loop, in contrast to the amplitude control loop, has to correct only phase errors, in an ideal case non-existent. Again the complexity of Fig.3 is misleading, all functions are shown explicitly for clarity.

The amplifier in Fig.3 differs from the amplifier in Fig.2 by the following. A phase detector PD is driven at one of its inputs from the Attenuator via Limiter 4. Limiter 4 erases the amplitude modulation $q(t)$ but maintains the desired phase modulation $\phi(t)$ as well as any parasitic phase modulation of output voltage $v$. The other input of phase detector PD is
driven via a voltage controlled Delay Circuit from Limiter 1. The Delay Circuit's range is >360° of the rf cycle and it is controlled by the output of the Integrator. The integrator is driven by the output of phase detector PD. The resulting control loop drives the static phase difference between the two inputs of phase detector PD to zero. Because the Delay Circuit tracks only slowly changing phase difference and both inputs of phase detector PD include the desired phase modulation \( \phi(t) \), the phase difference \( \phi(t) \) seen by phase detector PD consists only of fast dynamic phase errors, if any. Phase difference \( \phi(t) \) includes also the phase errors of Limiters 1 and 4 which must be held negligibly small for proper operation of the phase correction. The output of phase detector PD is also applied to the Low Pass Filter and results in an error voltage \( v_e \) following \( \phi(t) \). The bandwidth of \( v_e \) is in the worst case a low multiple of the bandwidth of the desired amplitude and phase modulation \( q(t) \) and \( \phi(t) \), i.e. much lower than the operating rf frequency \( \omega \). Thus to implement the Low Pass Filter that passes \( v_e \) but blocks the rf ripple at the output of phase detector PD is easy. Voltage \( v_e \) is amplified by error amplifier OA2 with complementary outputs W and Z carrying voltages \( v_w \) and \( v_z \) respectively. Signals \( v_w \) and \( v_z \) are both summed with voltage \( v_x \) in summing circuits S3 and S4. Multiplier M1 of Fig.2 has been divided into two multipliers, M1 and M3. The baseband input of multiplier M1 is driven by output voltage \( v_x \) of summing circuit S3. Similarly, the baseband input of multiplier M3 is driven by output voltage \( v_y \) of summing circuit S4. Inverting amplifier "-1" has been relocated from the output of multiplier M1 to the input of multiplier M3. Multiplier M2 is operating as in Fig.2, its baseband input is \( v_y \), its output \( v_M2 \) is driving the second inputs of summing circuits S1 and S2.

In Fig.3 a difference between the input and output envelopes will increase phasor \( v_M2 \) and decrease both phasors \( v_M1 \) and \( v_M3 \), or vice versa. This is causing, similarly to Fig.2, a correcting change in \( q(t) \). But in Fig.3 a voltage \( v_e \) caused by a phase error \( \phi \) will change \( v_M1 \) and \( v_M2 \) in opposite ways, thus rotating both \( v_1 \) and \( v_2 \) in a direction counteracting the phase error \( \phi \). This is illustrated in Fig.3a, where the assumption of \( v_w < v_e \) leads to \( v_M1 < v_M3 \). Since the phase correcting rotation will not be necessarily the same for vectors \( v_1 \) and \( v_2 \), a second order change in amplitude of \( v \) will result. It will be corrected by the amplitude control loop. The phase correction split angle \( \alpha \) of Fig.2a into two unequal angles \( \alpha_1 \) and \( \alpha_2 \) in Fig.3a.

We need again to calculate the phase correction loop's change in open loop gain \( H_P \) to assess the difficulty of keeping the loop both effective and stable over the expected range of phase error \( \phi \) and amplitude modulation range \( q(t) \). We will assume that the phase modulation \( \phi(t) \) of input signal \( v_{in} \) is zero.

Let us denote the gain of amplifier OA2 as \( A_2 \). Then the voltage \( v_w \) at output W of amplifier OA2 will be \( A_2 v_e \). This voltage is added to \( v_x = V_o - A_1 v_\alpha \) from amplifier OA1 in summing circuit S3. The sum applied to multiplier M1 will be \( v_o - A_1 v_\alpha + A_2 v_e \). Similarly, the voltage at output Z of amplifier OA2 will be \( v_z = -A_2 v_e \). This voltage is added to \( v_z = V_o - A_1 v_\alpha \) from amplifier OA1 in summing circuit S4. The sum applied to multiplier M3 will be \( V_o - A_1 v_\alpha - A_2 v_e \). Because of the difference between the control voltages of multipliers M1
and M3, the magnitude of vectors \( v_{M1} \) and \( v_{M3} \) in Fig.3a will not be the same anymore. The voltage \( v_y \) at input of multiplier M2 is still \( v_y = V_o + A v_a \).

From Fig.3a:

\[
\tan \alpha_1 = \frac{v_{M1}}{v_{M2}} = \frac{(v_x + v_w)}{v_y} = \frac{(V_o - A_1 v_a + A_2 v_e)}{(V_o + A_1 v_a)} \tag{7}
\]

and:

\[
\tan \alpha_2 = \frac{v_{M3}}{v_{M2}} = \frac{(v_x + v_2)}{v_y} = \frac{(V_o - A_1 v_a - A_2 v_e)}{(V_o + A_1 v_a)} \tag{8}
\]

By recalling that \( A_1 v_a / V_o = p \) and by introducing \( A_2 v_e / V_o = b \) we get:

\[
\alpha_1 = \arctan \left( \frac{1 - p + b}{1 + p} \right) \quad \text{and} \quad \alpha_2 = \arctan \left( \frac{1 - p - b}{1 + p} \right) \tag{9}
\]

With vector \( v_1 \) leading by phase angle \( \alpha_1 \) and vector \( v_2 \) lagging by phase angle \( \alpha_2 \), the voltage \( v \) at the output of the Power Combiner will have a phase shift \( e \) induced by error voltage \( v_e \):

\[
e = \frac{\alpha_1 - \alpha_2}{2} = \left( \arctan \left( \frac{1 - p + b}{1 + p} \right) - \arctan \left( \frac{1 - p - b}{1 + p} \right) \right) / 2 \tag{10}\]

This phase shift \( e \) will counteract the phase error \( \phi \).

We will now calculate the relative change of open loop gain \( H_p \) of the phase correction loop over the modulation range of \( q(t) = 0.1 \) to \( q(t) = 0.9 \). Let \( k \) be the sensitivity of phase detector PD and the Low Pass Filter (in volts/A\( \phi \)). Cutting the loop at the input of amplifier OA2, the open loop gain is \( H_p = k \text{d}e / \text{d}v_e \). With \( k, A_2 \) and \( V_o \) being constants, we can substitute for relative changes \( H_p = \text{d}e / \text{d}b \).

Graph 3 depicts \( e \) vs. \( b \) with \( q(t) \) as a parameter. The range of \( b \) is from -1 to 1. The slope of \( e \) vs. \( b \) is a strong function of \( q(t) \). Graph 4 depicts loop gain \( H_p = \text{d}e / \text{d}b \) vs. \( b \), again with \( q(t) \) as a parameter. We can see that over the range of \(-1 < b < 1\) the largest variation of loop gain \( H_p \) does not exceed 25% at any fixed \( q(t) \). Graph 5 depicts the range of \( e \) for \( b \) changing from \( b = -1 \) to \( b = 1 \) vs. \( q(t) \) which is a linearized measure of \( H_p \). The graph shows that the range of \( e \) is approximately proportional to \( q(t) \) up to \( q(t) = 0.8 \) with a maximum range of 64° (i.e. ±32°) at \( q(t) = 0.9 \).

In the amplifier of Fig.3 the open loop gain \( H_p \) as well as the range of achievable phase correction \( e \) is a very strong function of amplitude modulation \( q(t) \). It is possible that for some modulation schemes the sensitivity to or the range of potential phase errors will be directly dependent on output signal amplitude. In that case an almost direct proportionality of phase correction loop gain \( H_p \) on \( q(t) \) would not be a problem. However, if this is not
the case, the dependence of \( H_p \) on \( q(t) \) could be compensated by making the gain \( A_2 \) of amplifier OA2 inversely proportional to \( q(t) \), for example, by using voltage \( v_{b2} \) or preferably \( v_{b1} \) as a gain control signal.

2.2.2 Phase Correction Version 2

Another way of making phase correction loop gain \( H_p \) less dependent on \( q(t) \) is by changing both inputs of both summing circuits \( S_1 \) and \( S_2 \) by output voltages \( v_w \) and \( v_z \) of amplifier OA2. This is shown in Fig.4.

In Fig.4 the multiplier \( M_2 \) of Fig.3 is divided into two multipliers, \( M_2 \) and \( M_4 \). Multiplier \( M_2 \) is driving summing circuit \( S_1 \), and multiplier \( M_4 \) is driving summing circuit \( S_2 \). The baseband input of \( M_2 \) is now the voltage \( v_y + v_z \) supplied by summing circuit \( S_6 \), the baseband input of \( M_4 \) is the voltage \( v_y + v_w \) supplied by summing circuit \( S_5 \). This connection is chosen so that the output voltages \( v_x, v_y \) and the output voltages \( v_w, v_z \) change the magnitude of input voltages of summing circuits \( S_1 \) and \( S_2 \) according to the following table:

<table>
<thead>
<tr>
<th>( v_y - v_x )</th>
<th>( v_M2 )</th>
<th>( v_M4 )</th>
<th>( v_M1 )</th>
<th>( v_M3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( &gt;0 )</td>
<td>+</td>
<td>+</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>( &lt;0 )</td>
<td>-</td>
<td>-</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>( v_w - v_z )</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>( &lt;0 )</td>
<td>+</td>
<td>-</td>
<td>-</td>
<td>+</td>
</tr>
</tbody>
</table>

Fig.4a illustrates a situation where \( v_w - v_z < 0 \) leads to \( v_{M4} < v_{M2} \) and \( v_{M1} < v_{M3} \).

From Fig.4a:

\[
\tan \alpha_1 = \frac{v_{M1}}{v_{M2}} = \frac{(v_x + v_w)}{(v_y + v_z)} = \frac{(V_o - A_1 v_a + A_2 v_e)}{(V_o + A_1 v_a - A_2 v_e)} \tag{11}
\]

and:

\[
\tan \alpha_2 = \frac{v_{M3}}{v_{M4}} = \frac{(v_x + v_z)}{(v_y + v_w)} = \frac{(V_o - A_1 v_a - A_2 v_e)}{(V_o + A_1 v_a + A_2 v_e)} \tag{12}
\]

By recalling that \( A_1 v_a/V_o = p \) and \( A_2 v_e/V_o = b \) we get:

\[
\alpha_1 = \arctan \frac{1 - p + b}{1 + p - b} \quad \text{and} \quad \alpha_2 = \arctan \frac{1 - p - b}{1 + p + b} \tag{13}
\]

The change \( e \) in the phase of output voltage \( v \) will be:

\[
e = \frac{\alpha_1 - \alpha_2}{2} = \left( \frac{\arctan \frac{1 - p + b}{1 + p - b} - \arctan \frac{1 - p - b}{1 + p + b}}{2} \right) \tag{14}
\]
Graph 6 depicts again $e$ vs. $b$ with $q(t)$ as a parameter. The range of $b$ is from -1 to 1, which for values of $0.1 < q(t) < 0.9$ gives a range of $e$ of at least $\pm 26^\circ$. Graph 7 depicts open loop gain $H_p = \frac{de}{db}$ vs. $b$, again with $q(t)$ as a parameter. We can see that over the range of $-1 < b < 1$ and the range of $0.1 < q(t) < 0.9$ the worst case variation of open loop gain $H_p$ is 3:1. This variation of gain is compatible with keeping the phase correction loop effective but stable.

Graph 8 depicts the range of $e$ for $b$ changing from $b=-1$ to $b=1$ vs. $q(t)$ which is a linearized measure of $H_p$. The graph shows that the range of $e$ changes from $52^\circ$ (i.e. $\pm 26^\circ$) at $q(t)=0.1$ to $90^\circ$ (i.e. $\pm 45^\circ$) at $q(t)=0.7$, a less than 2:1 variation.

### 2.2.3 Crosstalk Between the Loops

To keep the phase correction loop from interfering with the amplitude modulation loop, $q(t)$ as a function of $p=A_1 v_a/V_o$ should be independent of $b=A_2 v_e/V_o$.

To keep the amplitude modulation loop from interfering with the phase correction loop, $e$ as a function of $b=A_2 v_e/V_o$ should be independent of $p=A_1 v_a/V_o$.

The two loops would be free of crosstalk if the multipliers $M_1$ to $M_4$ were driven with baseband control voltages proportional to the sine and cosine of $\alpha_1$ and $\alpha_2$. But because the voltages controlling the multipliers are derived in a simplified way in Fig.3 and in a somewhat less simplified way in Fig.4, it is important to check the amount of crosstalk between the amplitude modulation and phase correction loop.

#### 2.2.3.1 Influence of Amplitude Modulation on Phase Correction Loop

We will derive how much change will be required in phase loop error voltage $v_e$ to maintain a given phase correction $e$ as the modulation $q(t)$ is changing. The required change in $v_e$ can be read off Graphs 3 (for amplifier in Fig.3) and Graph 6 (for amplifier in Fig.4) by observing at any fixed value of $e$ the change in $b=A_2 v_e/V_o$ as parameter $q(t)$ is varied from $q(t)=0.1$ to $q(t)=0.9$. As could be expected, in the amplifier of Fig.3 the interaction is very strong at low values of $q(t)$, where the phase correction loop's open loop gain is at its minimum.

In the amplifier of Fig.4 the situation is much better, the worst case occurs at $e=\pm 26^\circ$ with a variation of $q(t)$ between 0.1 and 0.7. This requires a 1:2 change in $b$ and thus in error voltage $v_e$. But because gain $A_2$ of amplifier OA2 must be high enough to generate $e=\pm 26^\circ$ at $q(t)=0.1$ with a negligibly small $v_e$, the influence of amplitude modulation on the phase correction accuracy in the amplifier of Fig.4 is also negligible.

#### 2.2.3.2 Influence of Phase Correction on Amplitude Loop

In this section we shall investigate how much change will be required in input voltage $v_a$ of amplifier OA1 to maintain a given modulation level $q(t)$ over the range of phase correction angles $e$. The required change in $v_a$ can be read off from Graphs 9 (for amplifier
in Fig.3) and Graph 10 (for amplifier in Fig.4) by observing at any fixed value of $q(t)$ the change in $p = A_1 v_1 / V_o$ as parameter $b$ is varied from $b = -1$ to $b = 1$. Graphs 9 and 10 were generated in the following way.

With the phase correction loop in action, the two voltages entering the Power Combiner are:

$$v_1 = V \sin[\alpha t + \varphi(t) + \alpha_1] \quad \text{and} \quad v_2 = V \sin[\alpha t + \varphi(t) - \alpha_2]$$

(15)

The phase angle between $v_1$ and $v_2$ will be $\alpha_1 + \alpha_2 = 2 \alpha_1$. Thus the amplitude of output voltage $v$ will be $V_{\text{max}} \cos \alpha_1$ or $V_{\text{max}} \sin \alpha_1$ depending whether output $v$ is derived by vectorially adding (averaging) or subtracting $v_1$ and $v_2$. In the following we will assume vector addition or vector averaging. With the phase correction loop in action:

$$q(t) = \cos\left(\frac{(\alpha_1 + \alpha_2)}{2}\right) = \cos\left[\left(\frac{\arctan\left(\frac{1-p+b}{1+p}\right) + \arctan\left(\frac{1-p-b}{1+p}\right)}{2}\right)\right]$$

(16)

for amplifier in Fig.3 (Graph 9), and

$$q(t) = \cos\left(\frac{(\alpha_1 + \alpha_2)}{2}\right) = \cos\left[\left(\frac{\arctan\left(\frac{1-p+b}{1+p-b}\right) + \arctan\left(\frac{1-p-b}{1+p+b}\right)}{2}\right)\right]$$

(17)

for amplifier in Fig.4 (Graph 10).

We see in both Graphs 9 and 10 that the change in $p$ (and thus the change in $v_\alpha$) at any level of $q(t)$ is small compared to the value of $v_\alpha$ required for changing $q(t)$ from 0.1 to 0.9. And because gain $A_1$ must be high enough to guarantee a negligible $v_\alpha$ for changing $q(t)$ over its full range, the influence of phase correction on amplitude modulation will be negligible too.

2.2.4 Phase Correction Version 3

A third possibility to achieve phase correction is shown in Fig.5. The amplitude modulation function in Fig.5 is identical to Fig.2. A voltage controlled Delay Circuit similar to the one in Fig.3 and 4 is inserted into the amplifier's forward path. Contrary to Fig.3 and 4, here the Delay Circuit operates fast enough to follow the dynamic phase error $\phi$. Phase detector PD measures the phase difference between the output $u_i$ of Limiter 1 and output $u_o$ of Limiter 4 and keeps it negligibly small by controlling the Delay Circuit via the Low Pass Filter and amplifier OA2. As in Fig.3 and 4, phase detector PD, the Low Pass Filter and amplifier OA2 must pass the bandwidth of the dynamic phase error $\phi$ and, as in Fig.3 and 4, they do not see the desired phase modulation $\varphi(t)$. In the
arrangement of Fig. 5 the modulation control loop and the phase correction loop have no first order interaction.

2.2.5 Phase Correction Version 4

In Fig. 6 the voltage controlled Delay Circuit of Fig. 5 is replaced by a voltage controlled oscillator VCO. It is now the VCO frequency which is controlled by phase detector PD via the Low Pass Filter and amplifier OA₂. The VCO's output phase is such that the phase difference between output \( u_i \) of Limiter 1 and output \( u_o \) of Limiter 4 is negligible. Contrary to Fig. 5, phase detector PD, the Low Pass Filter and amplifier OA₂ must here process not only the dynamic phase error \( \phi \) but also the desired phase modulation \( \varphi(t) \). This causes any phase tracking error to appear first order in the output voltage \( v \). The loop must be also equipped by some frequency control means (not shown in Fig. 6) required to bring at start up the VCO frequency sufficiently close to the carrier frequency \( \omega_0 \) for phase loop capture. Again, in Fig. 6 the modulation control loop and the phase control loop have no first order interaction.

The 90° phase shifter in Fig. 6 can be often replaced by a conveniently available 90° tap from the VCO.

3. The Power Combiner

This part of the report addresses the Power Combiner required for changing the two constant envelope phase modulated carriers \( v_1 \) and \( v_2 \) into the desired amplitude and phase modulated output carrier \( v = q(t)V_{\text{max}} \cos(\omega t + \varphi(t)) \).

There are two conditions a Power Combiner must meet:

a) The Power Combiner must consist of reactive components only, so that no power is dissipated in the combiner itself.

b) To maximize overall power efficiency, the combiner must present a unity power factor (i.e. a resistive only) load to the two constant envelope output stages at all \( q(t) \), i.e. at all phase angles \( \alpha \). In case the constant envelope carriers \( v_1 \) and \( v_2 \) are supplied by class C transistor stages, this guarantees that at all phase angles \( \alpha \) the voltage between the transistors' emitter and collector is at its minimum value when the transistors conduct maximum current. Violation of this rule will cause excessive power dissipation in the transistors, thus reducing the efficiency of class C output stages.
3.1 Previously Published Combiners

To our knowledge, no combiner satisfying the above conditions a) and b) was yet published. The closest is a combiner described in [1], depicted here in Fig.7. This combiner offers an acceptable unity power factor for a limited range of conditions only, and the power factor rapidly falls to zero for $\alpha>72^\circ$ (assuming $v$ is generated by summation of phasors $v_1$ and $v_2$). This restricts the range of output amplitudes that can be supplied by the amplifier and sacrifices efficiency even within that range. Resistor R in Fig.7 represents the load, inductors $L_1$ and $L_2$ are uncoupled, the range of acceptable power factor is optimized by choosing capacitors $C_1$ and $C_2$.

3.2 The New Combiner

The new combiner in its most elementary form is depicted in Fig.8. It shows the voltage sources of $v_1$ and $v_2$, a transformer $Tr$ with a single center tapped winding, the desired load $R$ (e.g. the antenna), and two reactive loads, $X_1$ and $X_2$. The currents loading the voltage sources are $i_1$ and $i_2$, the current taken by the load is $i_R$, the current through the reactive loads are $i_{X_1}$ and $i_{X_2}$ respectively. The voltage across load $R$ is $v_R$. In all of the following discussion we will assume again that the bandwidth of phase modulations $\alpha$ and $\varphi(t)$ is only a small fraction of the carrier frequency $\omega$. The new combiner generates the output voltage $v_R$ as the vector average of voltages $v_1$ and $v_2$.

A phasor diagram of the voltages of the combiner in Fig.8 is shown in Fig.9. With phase modulation $\varphi(t)$ applied to both $v_1$ and $v_2$ equally and expected to appear also in $v$, we can assume that the reference zero phase in Fig.9 is phase modulated by $\varphi(t)$ and thus neglect $\varphi(t)$ in all further discussion. Both voltages $v_1$ and $v_2$ can be decomposed into two components. One is of common mode phase (vertical in Fig.9) creating the same voltage on all three nodes of transformer $Tr$ and acting as $v_R$ across load $R$. The other is of differential mode phase ($v_{diff}$ and $-v_{diff}$ in Fig.9) acting across transformer $Tr$. The amplitude of the common mode components acting across $R$ will be $v_R = V\cos \alpha$, the magnitude of each of the differential mode components will be $v_{diff} = V\sin \alpha$. The two common mode components will generate a current $i_R$ of amplitude $V\cos \alpha R$ flowing in $R$. The differential mode components will generate zero voltage across $R$ and no current in the transformer because of its assumed infinite impedance at frequency $\omega$. Each of the two voltage sources delivers half of the current through $R$, i.e. currents $i_{R1}=i_{R2}=i_R/2$ of amplitude $I_R/2=V\cos \alpha/(2R)$ and of common mode phase. Thus, if we first neglect currents $i_{X_1}$ and $i_{X_2}$ into reactances $X_1$ and $X_2$, the phase angles between the voltages $v_1$, $v_2$ and currents $i_1$, $i_2$ are $-\alpha$ and $\alpha$ respectively. The power factor seen by voltage sources $v_1$ and $v_2$ is $\cos \alpha$. For $\alpha$ approaching $90^\circ$ the power factor approaches zero.

We will now consider the reactances $X_1$ and $X_2$. The phasor diagram in Fig.10 shows the situation for voltage source $v_1$, the situation for source $v_2$ is similar. Fig.10 shows $v_1$, current $i_{R1}$ delivered by source $v_1$ (lagging $v_1$ by $\alpha$), and current $i_{X1}$ that is also delivered by source
As dictated by the reactive character of \( X_1 \), current \( i_{X_1} \) is in quadrature with \( v_1 \). Vector addition of current \( i_{X_1} \) with current \( i_{R1} \) results in a total current \( i_I \). If now reactance \( X_1 \) is properly chosen, \( i_I \) will be in phase with \( v_1 \), thus ensuring a unity power factor. To maintain unity power factor for all values of \( \alpha \), current \( i_{X_1} \), and thus reactance \( X_1 \) must be a function of \( \alpha \).

By observation of the phasor diagram in Fig. 10 we see that in order to keep \( i_I \) and \( v_I \) in phase, the amplitude \( I_{X_1} \) of current \( i_{X_1} \) must follow the amplitude \( I_{R1}/2 \) of current \( i_{R1} \) as follows:

\[
I_{X_1} = \frac{I_R \sin \alpha}{2}, \quad \text{and with} \quad I_R = \frac{V \cos \alpha}{R} \quad \text{we can write:} \tag{18}
\]

\[
I_{X_1} = \frac{V \sin \alpha \cos \alpha}{2R} = \frac{V}{4R} \sin 2\alpha \tag{19}
\]

To produce the desired current \( i_{X_1} \) in Fig. 10, reactance \( X_1 \) must be capacitive and its magnitude must depend on phase angle \( \alpha \) as:

\[
X_1(\alpha) = 4R/\sin 2\alpha \tag{20}
\]

If \( \alpha \) changes from 0 to 90°, \( X_1 \) in Fig. 8 is infinite for \( \alpha = 0 \), capacitive 4R for \( \alpha = 45° \), and infinite again for \( \alpha = 90° \).

Similarly, to produce the desired current \( i_{X_2} \), reactance \( X_2 \) must be inductive and its magnitude must depend on phase angle \( \alpha \) as:

\[
X_2(\alpha) = 4R/\sin 2\alpha \tag{21}
\]

If \( \alpha \) changes from 0 to 90°, \( X_2 \) will be infinite for \( \alpha = 0 \), inductive 4R for \( \alpha = 45° \), and infinite again for \( \alpha = 90° \).

A possible implementation of reactances \( X_1 \) and \( X_2 \) allowing their magnitude to be changed between infinite and 4R is shown in Fig. 11. Load \( R \), transformer \( T_r \), sources of \( v_1 \) and \( v_2 \) are the same as in Fig. 8. Reactance \( X_1 \) is implemented by tuned circuit \( L_1C_1 \), reactance \( X_2 \) by tuned circuit \( L_2C_2 \). In Fig. 11 we can assume \( L_1 = L_2 = L \). Capacitors \( C_1 \) and \( C_2 \) are tunable, for example by using varactor diodes. When the circuits are tuned to resonate with the carrier frequency \( \omega \), they represent an infinite reactance. When capacitor \( C_1 \) is increased above its resonance value \( C_o \), tuned circuit \( L_1C_1 \) becomes a capacitive reactance. When capacitor \( C_2 \) is decreased below its resonant value \( C_o \), circuit \( L_2C_2 \) becomes an inductive reactance.

We can write for capacitor \( C_1 \) and \( C_2 \):

\[
C_1 = C_o + 1/(\omega X_1) = C_o + \sin 2\omega/(4\omega R), \quad \text{i.e.} \quad \Delta C_1/C_o = \sin 2\omega/(4\omega RC_o) \tag{22}
\]

\[
C_2 = C_o + 1/(\omega X_2) = C_o - \sin 2\omega/(4\omega R), \quad \text{i.e.} \quad \Delta C_2/C_o = -\sin 2\omega/(4\omega RC_o) \tag{23}
\]
The higher the $\omega RC_0$ product, the smaller the required fractional change of capacity.

Other possible ways of implementing the variable reactances $X_1$ and $X_2$ is by tuning the inductances $L_1$ and $L_2$.

Still another method is changing the voltage across $L_1$ and/or $C_1$ and across $L_2$ and/or $C_2$ to a varying percentage of $v_1$ and $v_2$ respectively.

3.2.1 Tuning for Unity Power Factor

As described above, to maintain for all values of $\alpha$ a unity power factor at the inputs of the Power Combiner, the generation of the function $\sin 2\alpha$ is required. The following describes means for producing a voltage proportional to $\sin 2\alpha$ applicable to the amplifiers shown in Fig. 2, 6 and 7. In those Figures, as $\alpha$ is changing from 0 to 90°, $v_x$ is changing from zero to $2V_o$ and $v_y$ is changing from $2V_o$ to zero. The $\sin 2\alpha$ function has zero value at $\alpha=0$ and $\alpha=90^\circ$ and has its peak at $\alpha=45^\circ$ when $v_x=v_y=V_o$. The $\sin 2\alpha$ function can be approximated, over the range of $\alpha=0$ to $\alpha=90^\circ$, by a full wave rectifier consisting of a matched differential pair $Q_1$ and $Q_2$ (see Fig. 12). The pair is connected as two emitter followers loaded by a common current sink. With the bases of $Q_1$ and $Q_2$ driven by voltages $v_x$ and $v_y$ properly scaled by resistor dividers $R_1$ and $R_2$, the common emitter voltage $v_c$ approximates the function $-\sin 2\alpha$ with some dc offset. Graph 11 depicts the match. The dividers scaling $v_x$ and $v_y$ are chosen so that the peak-to-peak swing on both bases is approximately 200mV. The value of common emitter current $I$ and the emitter area of $Q_1$ and $Q_2$ are first order not influencing the match. If a larger swing of $v_c$ is desired, the voltage swing at the bases of $Q_1$ and $Q_2$ can be increased with a proper number of diodes connected in series with the transistor emitters.

The circuitry described above generates a signal proportional to $\sin 2\alpha$. When combined with the appropriate additional circuitry, the proper tuning of the reactive elements could be achieved. For example, additional linearizing circuitry would be required if the tuning were done by varactors that are generally non-linear. This additional circuitry is not the subject of this report.

4. Summary

The report describes new linear power amplifiers that generate an amplitude and phase modulated carrier by combining two constant envelope carriers in a power combiner. The significance of this method is that the constant envelope carriers can be produced by efficient class C or E output stages. The advantages of the described amplifiers over most of previously published circuits is the inclusion of the output stages and of the power combiner into feedback loops linearizing the amplifier's amplitude and phase response. The described amplifiers are distinguished also by their simplicity.
A further contribution of the report is a new, inherently lossless power combiner offering on both of its inputs a unity power factor at all times. This maintains the high efficiency of the class C or E output stages at all modulation levels.

References:


Fig. 2a

Fig. 3
Fig. 3a

Fig. 4
Fig. 8

Fig. 9

Fig. 10
Graph 1

Graph 2

Open Amplitude Loop Gain $H_a$ vs. $q(t)$
Graph 3: \( e \) vs. \( b \) with \( q(t) \) as Parameter

Graph 4: \( Hp \) vs. \( b \) with \( q(t) \) as Parameter
De = \{e \text{ for } b=1\} - \{e \text{ for } b=-1\} \text{ vs. } q(t)

GRAPH 5

e vs. b with q(t) as Parameter

GRAPH 6
Hp vs. b with q(t) as Parameter

Graph 7

De = [e for b=-1] - [e for b=1] vs. q(t)

Graph 8
Graph 9

Graph 10
Combiner Control Voltage for Fig. 2.5.6

Graph 11